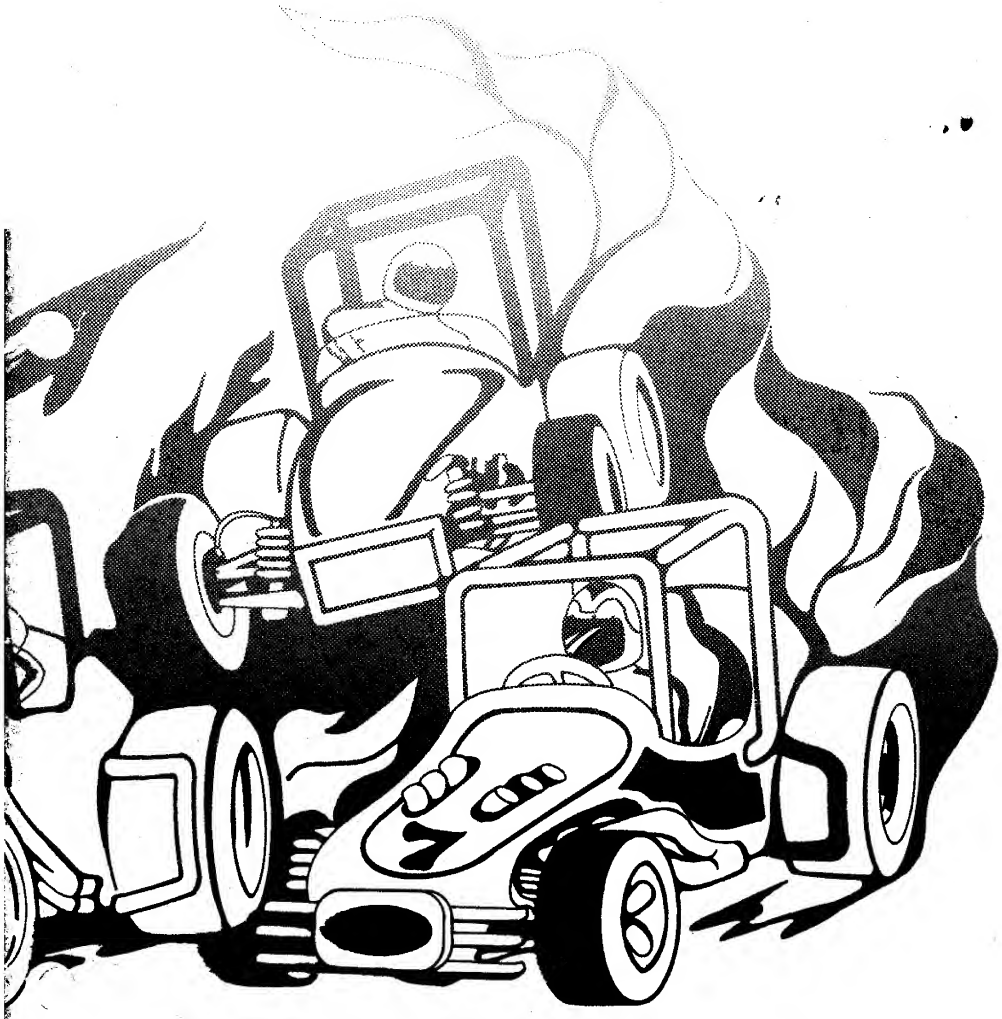
TM-078
1st printing

sprint 2™

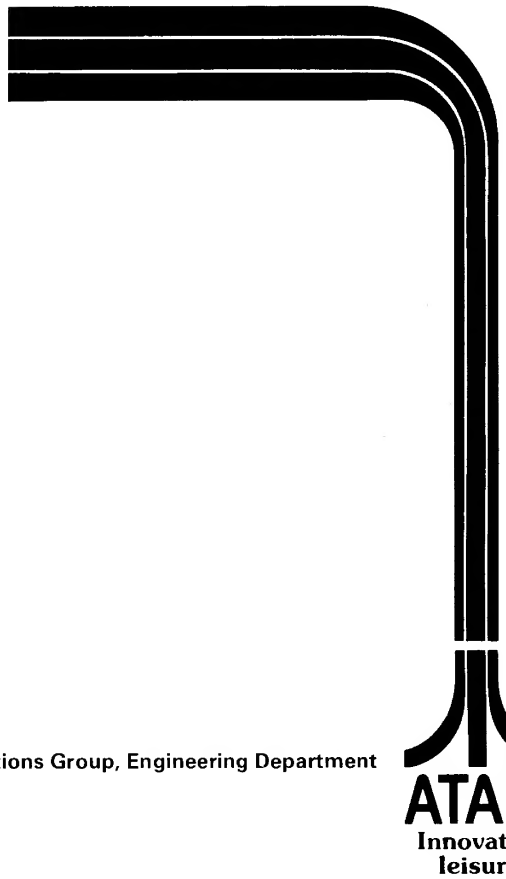
KEE GAMES
a wholly
owned subsidiary
of Atari, Inc

Operation, Maintenance and Service Manual



Operation, Maintenance and Service Manual

ATARI INC.
1265 BORREGAS AVENUE
SUNNYVALE, CA 94086
408/734-5310 • TELEX 35-7488



By the Publications Group, Engineering Department

Table of Contents

Table of Contents

I. INTRODUCTION

1.1 PHYSICAL DESCRIPTION OF GAME

Kee Games' Sprint 2 is a one or two player driving game. The game is packaged in its own distinctively-styled upright cabinet that rests directly on the floor. A 23-inch TV monitor is mounted in the top front of the cabinet, with the monitor viewing screen slightly tilted back from vertical. (Drawing number A006205-01, in Section IX of this manual, provides external and sectional views of the game cabinet.) The TV monitor viewing screen is covered with a plexiglas panel.

Player-operated controls are mounted side-by-side directly below the TV monitor viewing screen on the front of the game cabinet. The controls consist of two steering wheels, two four-speed gear shifters, two accelerator foot pedals, and three backlighted pushbutton switches. The switches are labeled TWO PLAYER START, TRACK SELECT, and ONE PLAYER START. A speaker mounted beneath each steering wheel provides game sound for the car controlled by that player.

Two identical coin mechanisms are mounted on the lower front center of the cabinet, below the steering and shifting controls. Either coin mechanisms can initiate play. The cash box is located behind a locked access door to the coin mechanisms.

1.2 SUMMARY OF GAME PLAY

The player's objective is to successfully keep his car in the boundaries of the race track and complete as many laps as possible before the end of game time. A single player operates the white car with the controls on the right side of the cabinet and competes with a black car and two grey cars. The black and grey cars are computer controlled. With two players, the player on the right operates the white car, the player on the left operates the black car, and the two grey cars are computer controlled.

After the proper coins have been inserted in the coin mechanism, the choice of which track to be played must be made. By pressing the TRACK SELECT pushbutton, the displayed tracks on the TV monitor screen are changed. The tracks become progressively more difficult each time the TRACK SELECT pushbutton is pressed, until the twelfth track is displayed, then the progression begins again from the easiest track.

Once the determination of the desired track is made, a player must press either the ONE PLAYER START or TWO PLAYER START pushbutton (dependent on the number of coins inserted in the coin mechanism). This begins the game play and the game timer starts counting down from 100.

Now with the left hand on the steering wheel, the right hand on the four-speed gear shifter, the right foot on the accelator foot pedal, and the sound of an idling motor, the player may begin to "drive" his car around the race track.

Acceleration is as in a real car. Start out in anything but first gear and the car accelerates slowly. Start out in first gear and the car accelerates nicely. Once the car is moving, shifting into progressively higher gears increases the speed of the car. If the car goes into a turn too rapidly, the car will go into a driver-controllable skid, with the sound of the skid on that player's speaker. Whenever a player's car comes in contact with any of the other three cars or an oil slick, the car goes into a semi-controllable skid. If a player's car makes contact with the track boundary, a crash sound will be heard and the car will stop.

By passing through check point areas on the track, a score is tallied at the top of the TV monitor screen. There are ten points awarded for the completion of each lap. However, the scoring point locations are not identified on the displayed track.

Thus the outstanding feature of Sprint 2 is that it is a highly competitive game. One player competes with himself and three "computer" controlled cars. Two players compete with themselves, each other, and with two "computer" controlled cars.

II. SPECIFICATIONS

2.1 GENERAL

Cabinet Dimensions:	Height 66¾ inches, Width 36 inches, Depth 31 inches.
TV Monitor:	Black and white, 23-inch screen, with composite video input.
Coin Mechanisms:	Two identical mechanisms, accept only quarters.
Cash Box:	Removable; located behind locked access door to coin mechanisms.
Power Cord:	Approximately 6 foot long, extending from rear of game cabinet and having grounded three-prong plug for conventional wall outlets.
ON/OFF Switch:	Hidden above the accelerator foot pedal on right side of game cabinet, for owner/operator access.
SELF/TEST Switch:	Located at the inside front of game cabinet to the immediate left of coin box.
Lighting:	One 24-inch fluorescent tube for cabinet lighting. One GE #47 lamp for coin mechanism lighting.

2.2 ELECTRICAL

Power Requirement:	Uses conventional grounded wall outlet providing 100 volts AC, 60 Hz, single phase, rated at about 200 watts.
Fusing:	All fuses accessable from rear access door of game cabinet; TV monitor has two 3AG 1-amp slow blow, 250 volt fuses and remainder of game is protected by one 3AG 3-amp quick blow, 250 volt fuses, mounted beneath the cover on the Electronics Assembly Tray.
Power Interrupt Switch:	These are safety interlock switches located inside the game cabinet rear access door. They cause the removal of AC power to the game when the access door is opened.

2.3 ENVIRONMENTAL

Operating and Storage Temperature Range:	From 32 degrees Fahrenheit to 120 degrees Fahrenheit (Ambient temperature).
Relative Humidity:	Maximum of 80% without condensation.

2.4 OWNER/OPERATOR OPTIONS FOR STRUCTURING OF GAME PLAY

Cost:	Free 25¢ for two players 25¢ per player 50¢ per player
Game length:	60 seconds 90 seconds 120 seconds 150 seconds
Extended Play:	None 30% of game length with PRO driving rating.
Miscellaneous:	No oil slicks Oil slicks Only easist track displayed during Attract Mode. Cycling of all twelve tracks during Attract Mode.

2.5 ACCESSORIES AVAILABLE ON SEPARATE ORDER

Video Probe:	Order from Atari
Universal Test Fixture:	Order from Atari, catalog no. CTF-1
Universal Test Fixture Sprint 2 Adaptor:	Buffer Board—Order from Atari, catalog no. 005822-01 Diagnostic Test Board—Order from Atari, catalog no. 005840-01

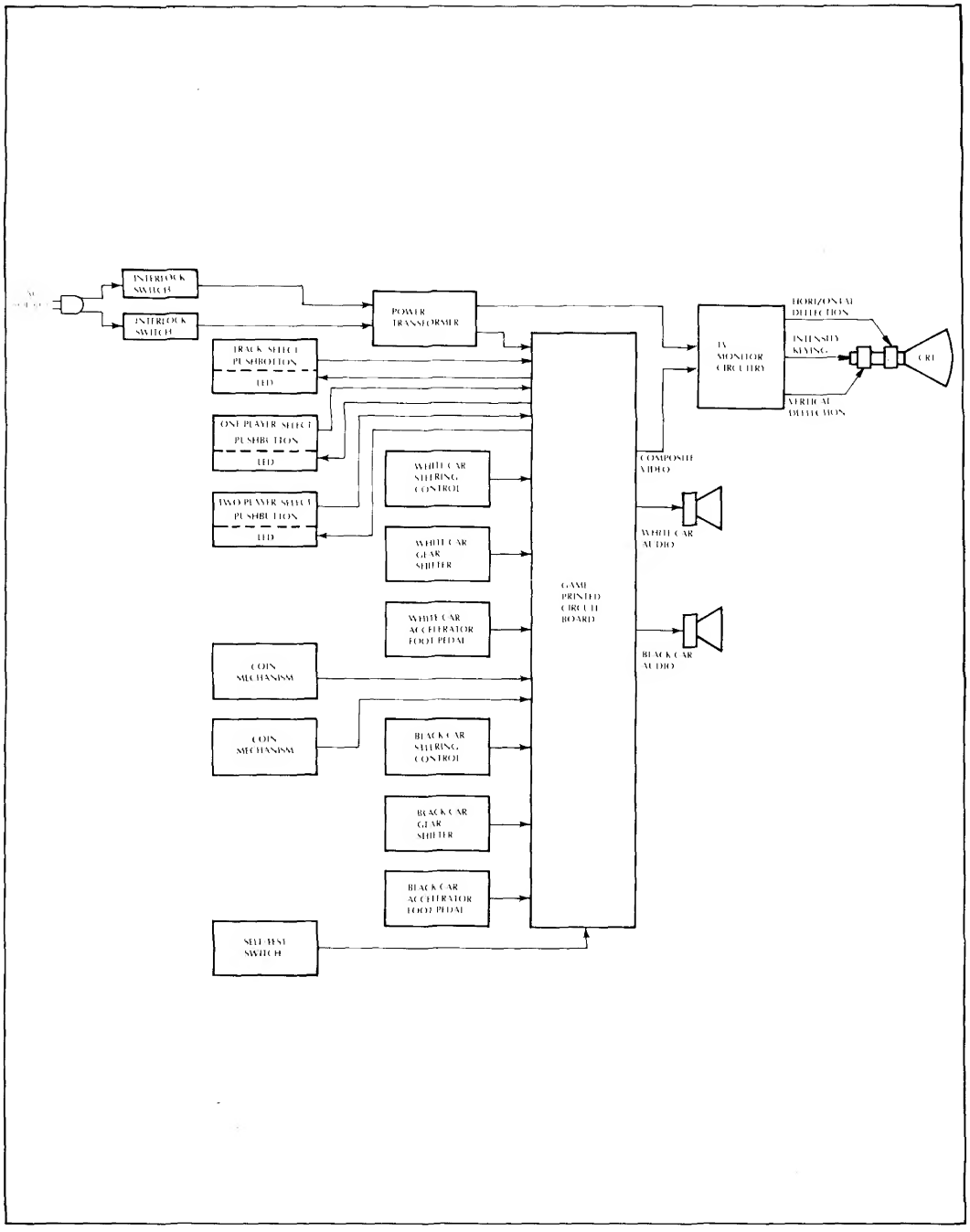


Figure 3-1 Functional Block Diagram of Sprint 2 Game

III. DESCRIPTION OF OPERATION

3.1 FUNCTIONAL DESCRIPTION OF GAME

The block diagram in Figure 3-1 illustrates the major functional parts of the Sprint 2 game. Note that the game printed circuit board (hereafter referred to as PCB) sends a composite video signal to the TV monitor and two separate audio signals to the speakers.

3.2 GENERAL INFORMATION

General information about the game in the following subparagraphs provides a background for the Installation Instructions in Section V of this manual, and the description of Game Sequence in paragraph 3.3 of this section.

3.2.1 Energizing the Game:

The game is energized by inserting the AC power plug into an active AC wall outlet that provides the specified AC power as listed in Section II, Specifications, of this manual. The Power ON/OFF" switch, hidden above the accelerator foot pedal on right side of game cabinet must be set to the "ON" position.

3.2.2 TV Monitor:

The game's TV monitor is a self-contained transistorized television monitor. Because the composite video signal sent to the monitor by the control circuitry differs in many respects from the signal derived from commercial TV broadcasts, the picture appearing on the screen is unlike that of a home TV set and the monitor does not produce any sound.

3.2.3 TV Monitor Picture:

Normally in black and white video games there are only two video levels, white and black. In Sprint 2 a grey video level is added to represent two programmed race cars. This is accomplished by using the video output summing resistors as a voltage divider during the grey car scans. The results is a decreased video output signal. Since the signal level determines the beam current of the TV monitor CRT, the result is a condition of not full on (white) and not full off (black) but somewhere between the two conditions (grey).

3.3 GAME SEQUENCE

3.3.1 Operating Modes:

During normal use, Sprint 2 can be described as operating in one of four modes; attract, ready-to-play, play, and freeze. Connecting the power cord to the proper AC source energizes the game and the game will be in the attract mode. The game remains in the attract mode until a coin has been inserted and the coins clear the coin mechanism, then the game goes into the start mode. After the desired track is selected by pressing the TRACK SELECT pushbutton, the play mode is initiated by pressing one of the player start pushbuttons; the game timer will begin counting down from 100 by one-digit increments. When the game timer reaches zero, the game goes into the freeze mode for approximately ten seconds before returning to the attract mode.

3.3.2 Attract Mode:

Figure 3-2 illustrates one of the TV monitor displays during the attract mode. During the attract mode, the four cars (one white, one black, and two grey cars) are displayed moving about the tracks as the tracks progressively change from the easiest to the most difficult (see Owner/Operator options, subparagraph 3.3.6 of this section). In this mode, there is no sound. It is normal, while the twelve tracks change, for some of the cars to "cheat" by going through some of the tracks' boundary lines. Across the top of the TV monitor one of the following will be displayed:

1 COIN PER PLAYER
2 COINS PER PLAYER
1 COIN PER 2 PLAYERS

3.3.3 Start Mode:

Figure 3-3 illustrates the TV monitor display during the start mode before the TRACK SELECT pushbutton is pressed.

The insertion of the proper coins in the coin mechanism initiates the start mode. When the coins clear the coin acceptor, the display will stop the automatic changing of the tracks and the easiest track is displayed and the cars are lined up at the starting line. Pressing the TRACK SELECT pushbutton, as instructed by the TV monitor display, will change the displayed track to the next more difficult track, until

the twelfth track is displayed. Pressing the TRACK SELECT pushbutton while the twelfth track is displayed will begin the cycle over again from the easiest track.

3.3.4 Play Mode:

The play mode is initiated by pressing the ONE PLAYER START or TWO PLAYER START pushbutton. As soon as the appropriate pushbutton is pressed, there will be a motor sound from each of the two speakers. The TV monitor display is the same as the start mode, except as follows; (1) the instruction words PUSH START BUTTON disappear from the bottom of the display; (2) the instruction words PUSH BUTTON TO CHANGE TRACKS disappear from above the track (only if the easiest track is displayed); and (3) the game timer begins counting down from 100. At the time of the initiation of the play mode, the player controls are enabled. As the player or players advance their cars around the track, a score for the player on the right is tallied beneath the word WHITE and a score for the player on the left is tallied under the word BLACK on the TV monitor display. Two points are awarded for passing each of the five checkpoint areas on the track. The five checkpoint areas are not identified on the TV monitor display.

3.3.5 Freeze Mode:

The freeze mode is initiated when the game timer reaches zero (see Owner/Operator Options, subparagraph 3.3.6 of this section). The TV monitor display is the same as in the play mode, except all car motion is "frozen," the words GAME OVER repeatedly appear and disappear across the top of the TV monitor display, and driver rating words GRANNY, ROOKIE, or PRO for each player appear at the bottom of the display. The freeze mode lasts for approximately ten seconds, then the game will go back into the attract mode.

3.3.6 Owner/Operator Options:

Options of the Sprint 2 game are available to the owner/operator for maximum player appeal for each game location. These options are listed in Table 3-1; they are preset for a certain game structure in the manufacturing process. To determine how the switches are set, place the self-test switch, located just inside and to the left of the coin mechanism of the game cabinet, to the ON position. At the end of the self-test sequence, the TV monitor will display the results of the toggle positions of switch assembly SW1, as listed in Table 3-1.

In order to change the toggle positions of the switch assembly, the Sprint 2 PCB must be removed from the RF Shield Box Assembly as described in Section VII, Dissassembly and Assembly, of this manual.

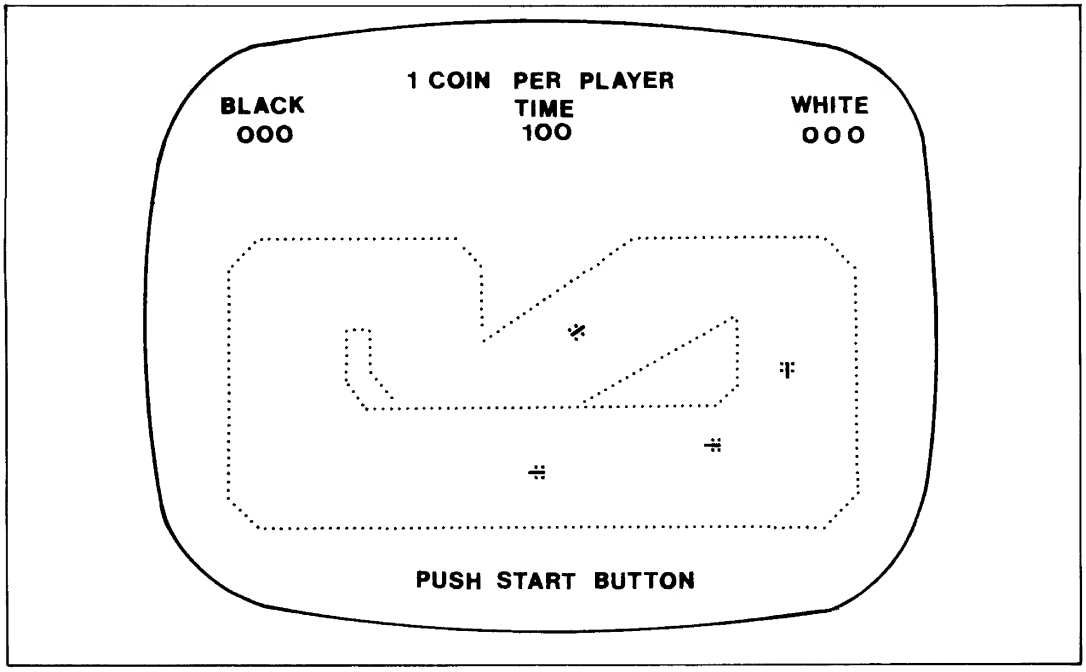


Figure 3-2 Attract Mode Display

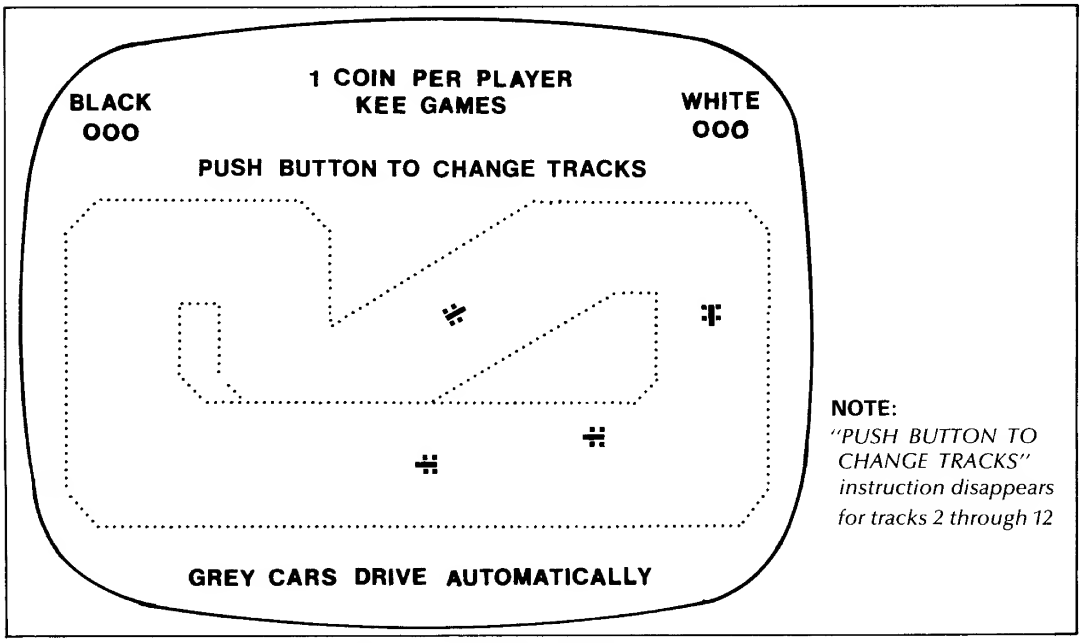


Figure 3-3 Ready-To-Play Mode Display

Table 3-1 Owner/Operator Optional Switch Settings

Switch Assembly SW Toggle Positions								TV Monitor Display	Description
1	2	3	4	5	6	7	8		
On								Oil	oil slicks added to tracks
Off									no oil slicks
	On								displays only easiest track during attract mode
	Off							Cycle	alternately displays all twelve tracks during attract mode
		On	On					1 coin per player	game cost 25¢ per player
		On	Off					2 players per coin	game cost 25¢ for two players
		Off	On					2 coins per player	game cost 50¢ for each player
		Off	Off					Demo	game is free (no attract mode)
				On				Extended play	extended play of 3/10 of time set by toggles 7 and 8, if player obtains pro rating in normal play
				Off					no extended play
					On				this toggle is not used, any position ok
					Off				this toggle is not used, any position ok
						On	On	Time 150	game time equals 150 seconds
						On	Off	Time 120	game time equals 120 seconds
						Off	On	Time 90	game time equals 90 seconds
						Off	Off	Time 60	game time equals 60 seconds

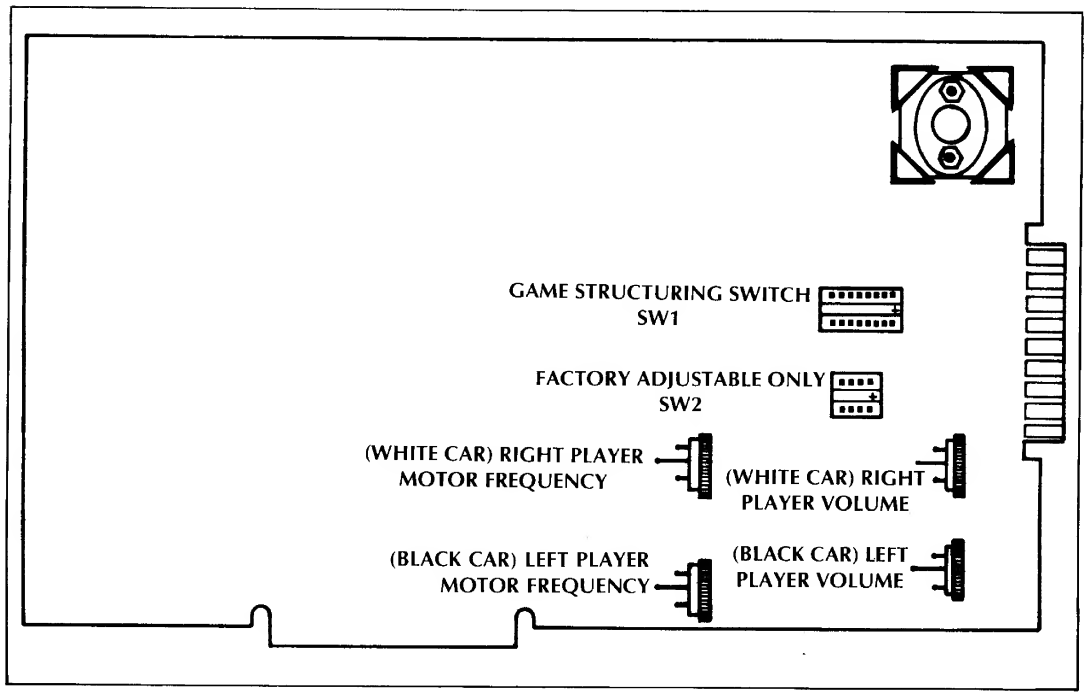


Figure 3-4 Location of Switch SW1 and Volume Controls

IV. THEORY OF OPERATION

4.1 GENERAL COMMENTS

This subsection provides a technical description of the Sprint 2 electronic circuitry. Section IX of this manual contains schematic diagrams, assembly drawings, and parts lists referred to in the following subparagraphs of this section.

On the Sprint 2 PCB schematic diagram, drawing number 005922, the symbol P (appearing at various inputs of the integrated circuits) indicates a connection to +5VDC through one of the pull-up resisters R1, R2, R4, R33, or R38.

For easy reference, the Sprint 2 PCB is divided into 126 sections. These sections are identified by letters A through R (skipping letters G, I, O, and Q because they may be easily confused with numbers 6, 1, and 0 respectively) for the short side of the PCB and numbers 1 through 9 for the long side of the PCB. For example, sheet 1 of 5 of drawing number 005922 illustrates a NAND buffer R9 at the upper left hand corner of the drawing. The component hardware of NAND buffer R9 will be found at coordinates R and 9 on the PCB.

The following circuitry discussion is separated into two sections; the microcomputer circuitry and the game circuitry. Figure 4-1 is a block diagram of the entire Sprint 2 PCB.

4.2 COMPONENTS OF THE MICROCOMPUTER SYSTEM

The microcomputer system carries out complex tasks of the game by performing a large number of simple tasks. Control of the system is the primary function of the Microprocessing Unit. The Microprocessing Unit causes the system to perform the desired operations by addressing the Program Memory for an instruction, reading that instruction, and then executing the simple task dictated by that instruction. Temporary storage of data necessary for the execution of future instructions, such as arithmetic operations, is stored into a Read/Write Memory.

4.2.1 Program Memory (Bottom Half of Schematic Sheet 3):

Program Memory consists of read-only memories (ROMs), permanently programmed by Kee Games to execute the Sprint 2 game. This memory has the capability of producing 8 bits of data for each of 8,192 combinations of ones and zeros on the 14 address inputs. In computer terminology, this is stated as a memory size of 8k x 8.

The Sprint 2 game contains one of three combinations of ROM chips to make up the Program Memory, depending on the dash number configuration of the Sprint 2 PCB. These combinations are listed in Table 4-1 and all combinations are illustrated on schematic sheet 3.

Since the data in the Program Memory is a permanent physical configuration of the ROM chips, the data is not lost when power is disconnected from the game or when the chip is removed from its socket. Since the Program consists of read-only memory, the result of an address input can only be the "reading" of data stored in the manufacturing process. It is not possible to "write" in more data.

4.2.2 Read/Write Memory (Top Half of Schematic Sheet 3):

Read/Write Memory (RAM) consists of random-access memory, which actually contains eight random-access memories (2102-1s). Data may be stored in the RAM (called "writing" the RAM), then

Table 4-1 ROM Combinations of Program Memory for Sprint 2 PCB Different Configurations

PCB Part No.	Sprint 2 PCB Location																			
	A0	C0	D0	E0	F0	F1	H0	H1	J0	J1	K0	K1	L0	L1	M0	M1	N0	N1	P0	P1
5922-01					X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
5922-02	X	X											X	X	X	X	X	X	X	X
5922-03	X	X	X	X																

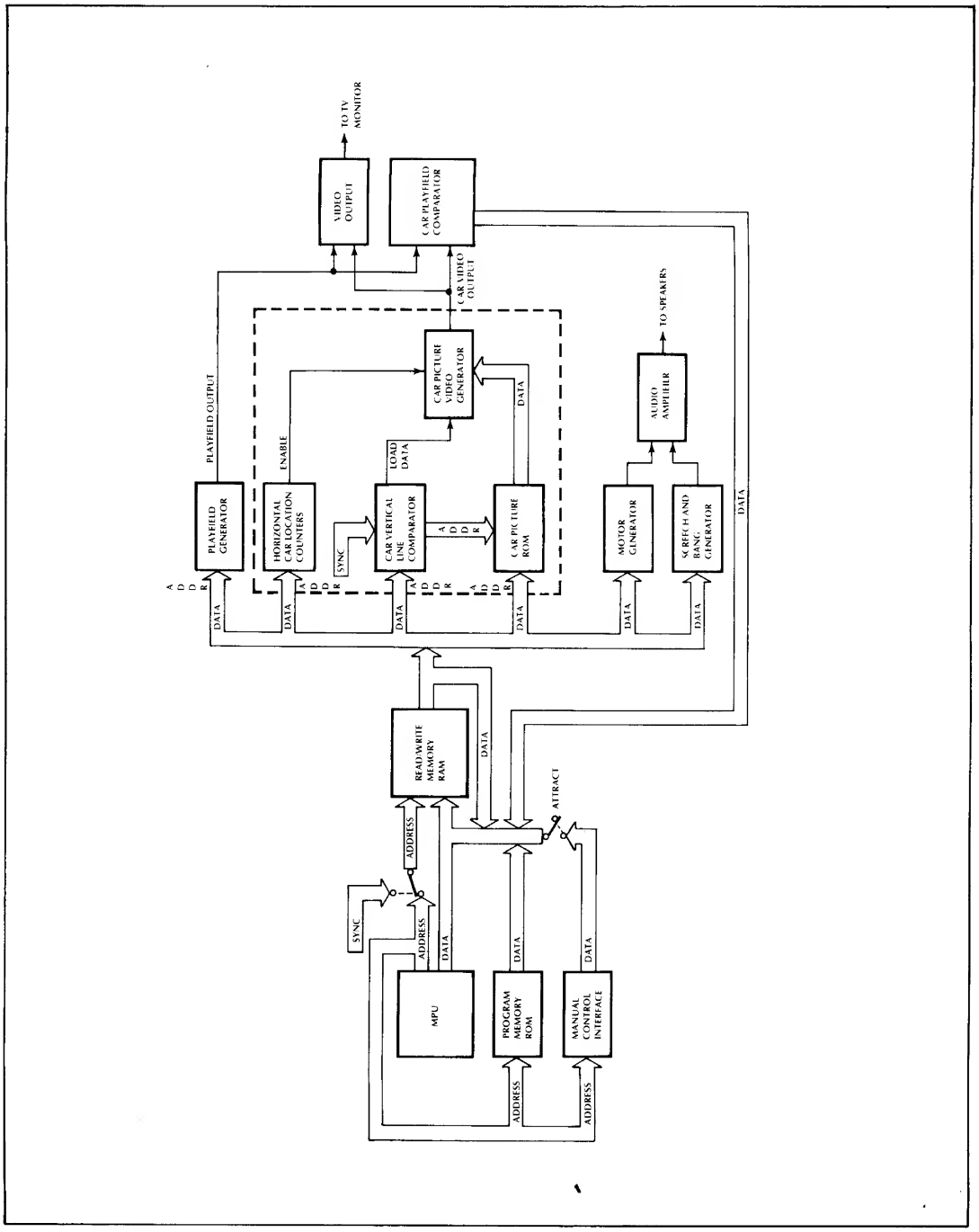


Figure 4-1 Sprint 2 PCB Block Diagram

later recalled (called "reading" the RAM). Memory size of the Read/Write Memory is 1k x 8.

In order to read from the RAM, R/$\overline{W}$ (pins 3) input of all random-access memories must be at a high logic level; to write into the RAM, R/$\overline{W}$ must be a low logic level.

As previously mentioned, data stored in the RAM is for the purpose of performing operations on data as instructed by the Program Memory. Since the RAM is a temporary storage area, removing power from the RAM chips will "erase" all stored data.

4.2.3 Microprocessing Unit:

As mentioned earlier, the controller of the microcomputer is the microprocessor (MPU). From the MPU, a sixteen-bit address bus addresses Program Memory, RAM, and an Address Decoder. An eight-bit bi-directional data bus serves as a path for transferring data from Program Memory and to and from the RAM and other interfacing devices.

4.2.4 Tri-State Devices:

Tri-state devices, such as E5 of schematic sheet 3, are capable of having normal logic output of ones and zeros when disable (pin 1) is at a low logic level. When disable is at a high logic level, the output becomes a high impedence. In other words, when disable is at a high logic level, it is equivalent to completely removing device E5 from the circuit. ROMs and RAMs are also tri-state devices. Each ROM or RAM must be enabled by a certain logic level at its chip-enable input before the device is capable of outputting or inputting data.

4.3 THE MICROCOMPUTER SYSTEM

The primary function of the Sprint 2 Microcomputer is to instruct the game circuitry for the proper TV monitor display and audio outputs for corresponding manual inputs.

4.3.1 Program Memory Enable:

With initial power applied to the Sprint 2 PCB, the MPU addresses Program Memory for an instruction by placing a 16-bit code at outputs AB0 through AB15. The address decoder, consisting of ROM E2, one-of-ten decoders D2, F2, and E8, and addressable latch A1, receives the five most significant bits of this address code (address 9 through 13) as an instruction of which part of Program Memory to access. Outputs of one-of-ten decoder F2 enable only the individual ROMs of Program Memory required for the desired instruction.

4.3.2 RAM Enable:

Now, with the Address Decoder addressed for the enabling of the desired Program Memory ROMs, and Program Memory addressed for a data instruction, the MPU receives an 8-bit data instruction from Program Memory on the data bus. If this data instruction includes the storage of information, the MPU addresses the RAM and writes the data into the memory RAMs. The procedure of writing into RAM is enabled by two signals; chip enable CE (pins 13) and R/$\overline{W}$ (read/write) (pins 3) of the RAM must be at a low logic level. The Address Decoder ROM (E2) receives an address (A9 through A13) and one-of-ten decoder D2 receives a high logic level write signal from the MPU. The results of these signals is a low logic level $\overline{DISPLAY}$ at the input of multiplexer K2 for a low logic level chip enable CE at pins 13 of the RAM. The MPU also causes the R/$\overline{W}$ (pins 3) input to the RAM to be pulsed, via the $\overline{WRITE}$ signal. When this input is pulled to a low logic level, MPU data on the data input to the RAM (pins 11) is stored into the RAM location determined by address inputs A0 through A9.

4.3.3 Phase 1 and Phase 2:

Phase 1(Φ1) and phase 2 (Φ2) are outputs of the MPU and are formed by shaping the pulse of horizontal synchronization pulse 4H by D-type flip-flop A7. The 4H input of A7 (pin 13) is fed twice through the flip-flop at a clock rate of 12.096 MHz. The output of the first flip-flop and the output of the second flip-flop is fed through an OR gate to produce a phase 0 (Φ0) signal, as illustrated in figure 4-2. The MPU provides an output of Φ2 that is exactly like Φ0, except with a slight delay, and an output Φ1 that is of an opposite phase of Φ2. Signal Φ2 is fed through AND gate N3, which acts as a buffer.

When Φ1 is positive, the address and data lines of the MPU change and stabilize for the next output. When Φ2 is positive, the MPU addresses memory on the address bus and inputs or outputs data on the data bus. In order to guarantee that the MPU data is written to external devices at the proper time, write enable (WRITE, A7 pin 10) is shaped by NAND gate A8 and D-type flip-flop A7 as illustrated in figure 4-3.

Phase 2 is also used to control the output of RAM Address Multiplexer K2, J2, and H2. The multiplexer acts as a 12-pole-double-throw-switch switched at a rate of Φ2. Again, as previously mentioned, the RAM is addressed by the MPU and data written into it when Φ2 is a high logic level. When Φ2 is at a low logic level the RAM is addressed by horintal and vertical synchronization and data is read out of the RAM.

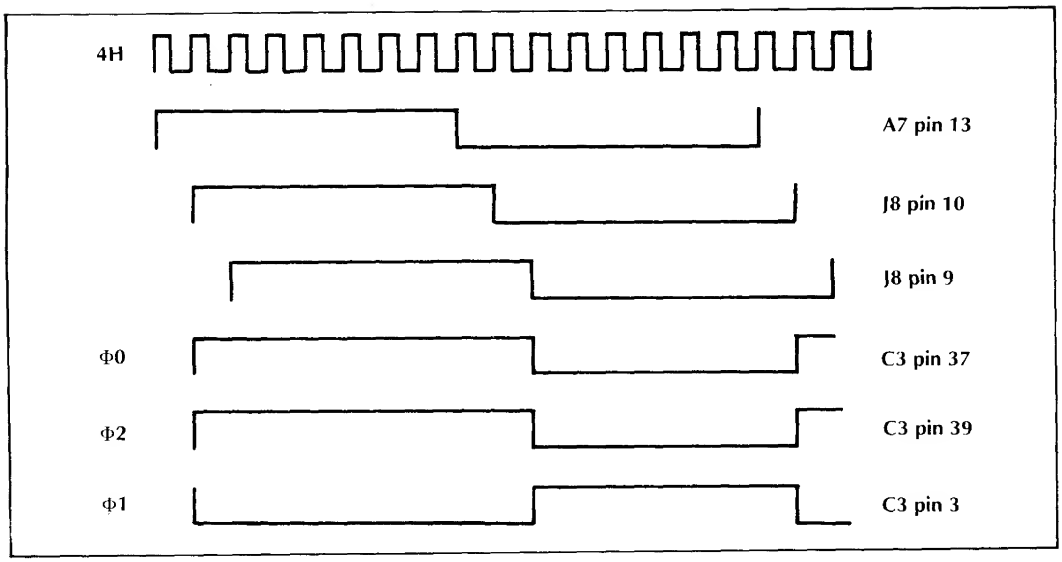


Figure 4-2 Phase 1 and Phase 2 Signal Shaping

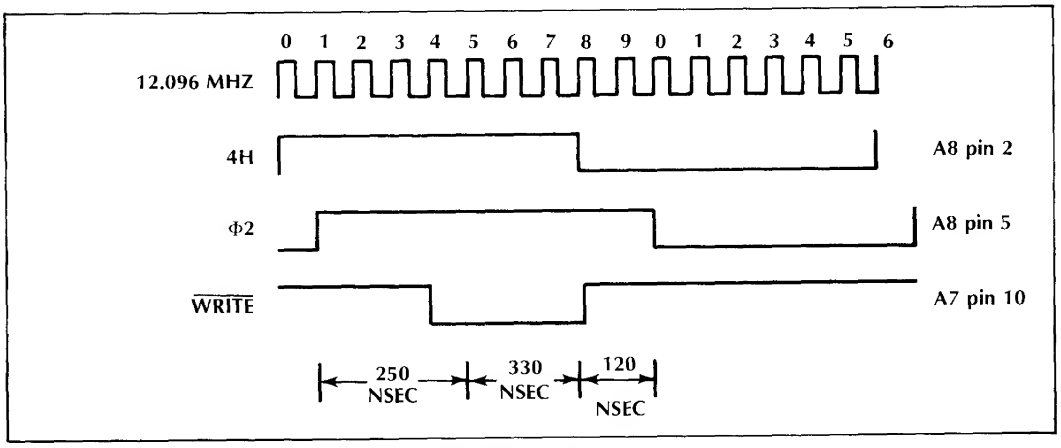


Figure 4-3 RAM Write Enable Signal Shaping

4.3.5 RAM Output:

The RAM has a second data output latch that places the RAM data at the output of D-type flip-flop F5 and L5 with the next rising edge of Φ2 (clock input of F5 and L5).

4.4 MICROCOMPUTER WATCH DOG

Watch dog is an external monitoring system that resets the Program Execution back to its initial instructions, if the program execution memory deviates from its intended sequence. This is accomplished by a watch dog statement (address code), incorporated in Program Memory, that results in a $\overline{\text{TIMER RESET}}$ pulse at the output of the Address Decoder. This reset pulse must occur before decade counter C6, 7 reaches the count of eight. Therefore if the Program Memory is functioning properly, a $\overline{\text{TIMER RESET}}$ pulse occurs within every eight frames of video.

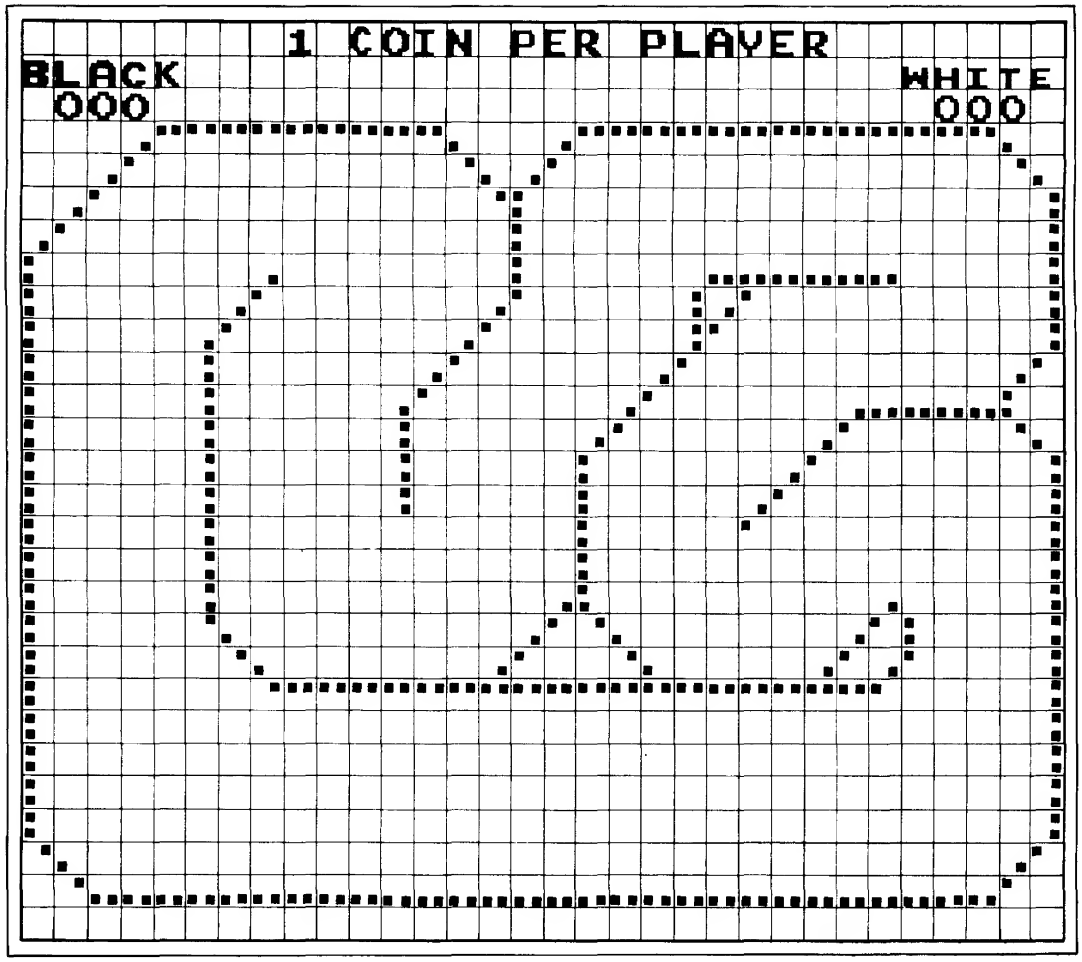


Figure 4-4 TV Monitor Playfield Display

4.5 COMPONENTS OF SPRINT 2 GAME CIRCUITRY

The game circuitry receives game instructions from the microcomputer and responds with the proper video and audio outputs. Manual controls of the game circuitry provide control information as a data input to the microcomputer.

4.5.1 System Clock and Sync Generator (Top of Schematic Sheet 1):

The crystal-controlled-clock generates a 12.096 MHz clock frequency that is used to produce all of the operating frequencies of the game. Insert 1, supplied with this manual, illustrates the horizontal and vertical sync synchronization waveforms. Note that 9-bit binary counter (R8, P8, and N8) counts from 128 to 512, accomplished by tying bit 128H (pin 5 of N8), to a pull-up resistor. Also note that the output of D-type flip-flop N2 is controlled by Sync PROM M2 (programmable read only Memory programmed by Kee Games for the desired output) for an output as illustrated by insert 1.

The horizontal and vertical synchronization signals are used to produce a TV monitor raster made up of 262 horizontal lines at a horizontal frequency of 15,750 Hz (256H). Synchronized with line 224 is a vertical blanking pulse that occurs for the duration of 38 more horizontal scans, resulting in the total number of 262 lines per frame.

4.5.2 Playfield Generator (Left Bottom of Schematic Sheet 1):

The Playfield Generator generates both the playfield and all alpha/numeric video for the TV monitor display. This is accomplished by the playfield ROM (consisting of ROMs P4 and R4 for a memory size of 512 x 8), shift register R3, and binary counter R2.

As illustrated in figure 4-4, the TV monitor display is made up of thirty-two horizontal by twenty-eight vertical grid sections. For each grid section, there is a byte of data (one byte equals eight bits D0 through D7) in the microcomputer RAM. During the Φ2 cycle, the RAM is addressed by the MPU, at which time the desired byte of data is transferred from Program Memory to the data input of the RAM. Then, during the Φ1 cycle, the horizontal and vertical synchronization signals can access each of these bytes of data as that particular grid is to be displayed. The RAM then outputs six bits of data (DISPLAY 0 through DISPLAY 5) that address any of the sixty-four different alpha-numerics and playfield characters stored in the Playfield ROM.

The Playfield ROM is programmed by Kee Games to provide eight bits of data for each of 512 addresses. The least significant addresses are from vertical synchronization 1V, 2V, and 4V and the 504 most significant addresses are DISPLAY 0 through DISPLAY 5 from the microcomputer RAM. For each of the 512 addresses, there is one of sixty-four grid pictures, each being eight scan lines high.

The top of figure 4-5 illustrates the letter "C" as it would be "traced" on the TV monitor display. The RAM would provide one six-bit address to the Playfield ROM for the letter, while vertical synchronization 1V, 2V, and 4V would complement the RAM address for each of the horizontal scan lines. The bottom of figure 4-5 illustrates the output of shift register R3 for each horizontal scan.

Note the letter "C" in grid section horizontal 11, vertical 1 in figure 4-4. In order to generate this character in this location, the microcomputer RAM would output a data code at the time this part of the display is being scanned. This six-bit code (DISPLAY 0 through DISPLAY 5) would contain the Playfield ROM address for the letter "C." Vertical synchronization 1V, 2V, and 4V would determine which of the eight lines of the character was being scanned at that time.

Shift register R3 then loads the actual playfield or alpha/numeric data from the playfield ROM and shifts it out in serial video (R3 pin 13).

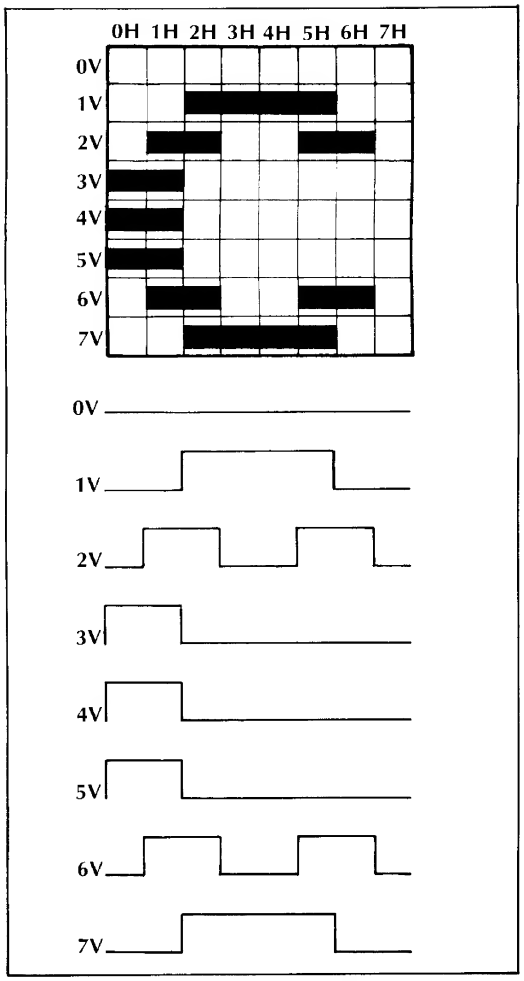


Figure 4-5 Playfield Generator Character Trace

Binary counter R2 latches data DISPLAY 7, from the microcomputer RAM. This results in the selection of white playfield video if DISPLAY 7 is a high logic level or black playfield video if DISPLAY 7 is a low logic level. In actuality, only some alpha/numerics and all oil slicks are represented in black video, while all of the racetrack boundary (playfield) is represented in white video.

Binary counter R2 is also used to produce the COMP SYNC*, COMP BLANK*, and a 256H* signal that are all delayed one character's width from their original timing. This delay is used to center the playfield on the monitor's horizontal scan.

4.5.3 Motion Generator (All of Schematic Sheet 2):

The motion generator generates the video for the four cars, which are the only moving objects of the Sprint 2 game. The car picture ROM (consisting of ROMs J6 and K6, for a memory size of 512 x 8) is programmed by Kee Games to provide sixteen bits of data for each of the eight lines of each of the thirty-two different states of rotation of a car.

The microcomputer RAM provides three words (bytes) of data for the display of each car picture. The first byte determines the vertical location of the car, the second determines the proper rotation picture of the car, and the third determines the horizontal location of the car. The accessing of these bytes of RAM data is done during the horizontal blanking period ($\overline{256H}$).

Vertical position data is received by Vertical Line Comparator M4 and L4. Take for example, the data code for a car to be displayed beginning on line 120. The RAM byte data code of 01111000 would be loaded into the comparator. When the vertical line comparator reaches the count of 01111000, and 8H, 64H, $\overline{256H}$, and Φ2 are all at a high logic level, the conditions are met for a low logic level at the output of NAND gate N4 (pin 8). One Φ2 clock pulse later, a low logic level appears at the Q3 (pin 7) output of latch L5 (clock input for L5 is located on schematic sheet 3). This initiates the eight vertical load pulses as illustrated in Insert 1, supplied with this manual.

The RAM byte data code that controls car rotation is capable of addressing any of thirty-two different car pictures. The five bits of data code necessary to do this (DISPLAY 3 through DISPLAY 7) are applied directly to the address input of the Car Picture ROM J6 and K6. The least significant address lines applied to the Car Picture ROM (inputs A0, A1, A2, and A3) complement the rotation data code by determining which of the eight lines of the car is being described by the ROM data output, and whether it is the first half (right) or second half (left) of the car to be displayed. When Φ2 is a high logic level, the video data output (VID 0 through VID 7) from the Car Picture ROM is timed with load vertical pulse LDVxB. Load vertical pulse LDVxB enables shift register M7 (K7, H7, or E7) to load the video data from the Car Picture ROM. This data is for the right half of the car.

When Φ2 is a low logic level, the video data output (VID 0 through VID 7) from the Car Picture ROM is timed with load vertical pulse LDVxA. Load vertical pulse LDVxA enables shift register N7 (L7, J7, or F7) to load the video data from the Car Picture ROM. This data is for the left half of the car.

Now to review, the Motion generator has received a RAM data code for where the car is to be displayed vertically and a RAM data code for the proper picture of the car. The final instruction needed is for the horizontal placement of the car. The RAM byte that determines this is received by the car horizontal location counter.

The car horizontal location counter R5 and R6 (P5 and P6, N5 and N6, or M5 and M6) is loaded each horizontal line by a load horizontal pulse LDHx as illustrated in Insert 1, supplied with this manual. The counter is preset to a given count by the RAM data code (DISPLAY 0 through DISPLAY 7) during horizontal blanking. At the end of horizontal blanking, 256H goes to a high logic level, and the counter is enabled to begin counting up at a clock rate of six MHz.

4.5.4 Video Output (Schematic Sheet 1):

The Video Output circuit receives all video signals and gates them together through summing resistors R48, R49, and R50. Cars 3 and 4, the grey cars, are gated through a parallel path to produce a positive signal through resistor R50 and a negative signal through R49. The summed result is between a full ON condition (white) and a full OFF condition (black) which is a grey level of the TV monitor display.

4.5.5 Car/Playfield Comparator (Top Center of Schematic Sheet 5):

The Car/Playfield Comparator is a network of logic gates that gate together the three video outputs of the Motion Generator and the two video outputs of the Playfield Generator. Table 4-2 provides the seven possible conditions that would cause a high logic level to appear on data lines D6 and D7 of the data bus. The microcomputer MPU recognizes an output from comparator if the MPU initiates an address to the Address Decoder for a $\overline{\text{COLLISION 1}}$ or $\overline{\text{COLLISION 2}}$ "read" signal. This causes tri-state devices E5 and E6 to be enabled and allows the output of the Car/Playfield Comparator to be transferred onto the MPU data bus.

When the MPU receives the data that a skid (high logic level on data line D6) or crash (high logic level on data line D7) condition exists, Program Memory instructs the MPU to cause the appropriate response to be displayed on the TV monitor display, and then to clear the Car/Playfield Comparator. This is done by the MPU outputting an address that is

decoded to cause a low logic level $\overline{\text{COLLISION RESET 1}}$ and/or $\overline{\text{COLLISION RESET 2}}$. The Collision Reset signals reset latch H6 of the Car/Playfield Comparator.

Table 4-2 Conditions of Car/Playfield Data Output

Car/Playfield Comparator Conditions	Data Line Output
Car 1 equals Car 2	D6
Car 1 equals Car 3 or 4	D6
Car 2 equals Car 3 or 4	D6
Car 1 equals Black Playfield (oil)	D6
Car 2 equals Black Playfield (oil)	D6
Car 1 equals White Playfield (track boundary)	D7
Car 2 equals White Playfield (track boundary)	D7

4.5.6 Manual Control Interface (Left Side of Schematic Sheet 5):

The main component of the Manual Control Interface is multiplexer M8. This component acts as a two-pole four-position switch, operated by address lines ADR6 and ADR7 from the microcomputer MPU. Table 4-3 lists the input/output relationship of multiplexer M8 with the given Address inputs. Multiplexer M8 interfaces three different sources of information as follows; 1) coin information; 2) steering information; and 3) switch information. All information is received by the microcomputer MPU when the MPU addresses the Address Decoder for a low logic level $\overline{\text{SWITCH}}$ signal that enables tri-state device K5 for a data output on the D6 and D7 data lines.

Coin information is a matter of storing in the microcomputer RAM the number of times a low logic level pulse appears on the data lines, when the appropriate address input of multiplexer M8 is being addressed. The microcomputer MPU only "looks" for coin pulses during the attract mode.

Steering information is "looked" for by the microcomputer MPU during the play mode. The steering printed circuit assembly consits of two light emitting diodes that are optically aligned with two light sensitive transistors. A toothed cylinder, that is turned by the steering wheel, is inserted between the light emitting diodes and the transistors, and interrupts the light from the diodes. When the steering wheel is turned, two pulses appear at the output of the steering printed circuit assembly that differ in phase. As illustrated in figure 4-6, when the wheel is turned to the right, the A output pulse leads the B output pulse. When the wheel is turned to the left the A output pulse lags the B output pulse. The inverse of the two pulses are applied to the D and clock inputs of two D-type flip-flops (see schematic). The microcomputer MPU recognizes that a steering maneuver has been made when a low logic level appears on data line D7. The MPU then "looks" at data line D6 and determines from the logic level (high or low) if "Steering A" input is leading or lagging "Steering B" input. Once the MPU has processed a steering maneuver, the MPU then outputs an address that is decoded by the Address Decoder and results in a low logic level $\overline{\text{STEERING RESET 1}}$ or $\overline{\text{STEERING RESET 2}}$ signal that resets the D-type flip-flop responsible for the steering signal.

Switch information is received by multiplexer M8 at inputs 1CO and 2CO. The microcomputer MPU addresses Decoders F9, H9, and J9 to determine if a switch is opened or closed. If closed a low

Table 4-3 Operation of Multiplexer M8 With Given Input Address

Address Logic Level		Output	
ADR6	ADR7	1Y (D7)	2Y (D6)
L	L	1C0	2C0
L	H	1C1	2C1
H	L	1C2	2C2
H	H	1C3	2C3

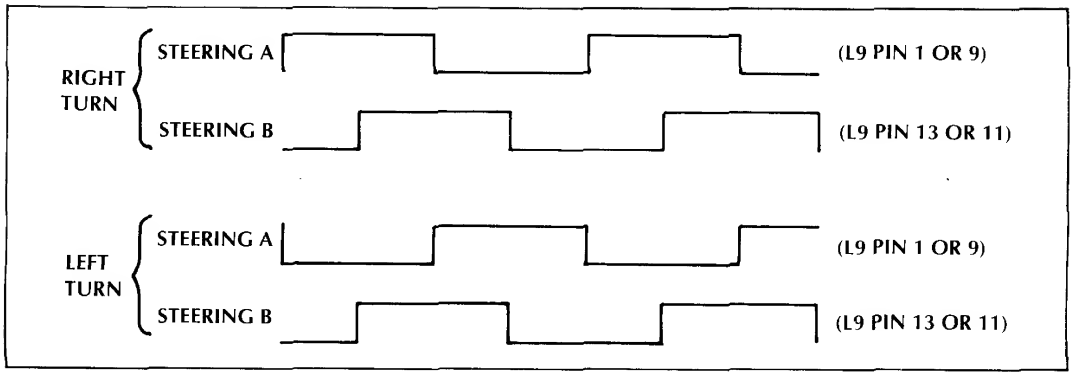


Figure 4-6 Steering Printed Circuit Assembly Output Pulses

Table 4-4 Addresses of Switch Positions for MPU Data Line D6 D7 Input

	0	1	2	3	4	5	6	0	1	2	3	4	5	6	0	1	2	3
ADR0	L	H	L	H	L	H	L	L	H	L	H	L	H	L	L	H	L	H
ADR1	L	L	H	H	L	L	H	L	L	H	H	L	L	H	L	L	H	H
ADR2	L	L	L	L	H	H	H	L	L	L	L	H	H	H	X	X	X	X
ADR3	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L
ADR4	H	H	H	H	H	H	H	L	L	L	L	L	L	L	H	H	H	H
ADR5	L	L	L	L	L	L	L	H	H	H	H	H	H	H	X	X	X	X
multiplexer M8 input 1CO (D7)	1ST1	1ST2	2ND1	2ND2	3RD1	3RD2		GAS1	GAS2	SELF TEST		START 1	START 2	TRACK SEL	OIL SLICK	$ MODE 1	EXT PLAY	TIME 1
multiplexer M8 input 2CO (D6)															TRK CYC	$ MODE 0	SPARE	TIME 0

NOTE: X indicates a condition of either high or low

logic level pulse will result for the given address as listed in table 4-4.

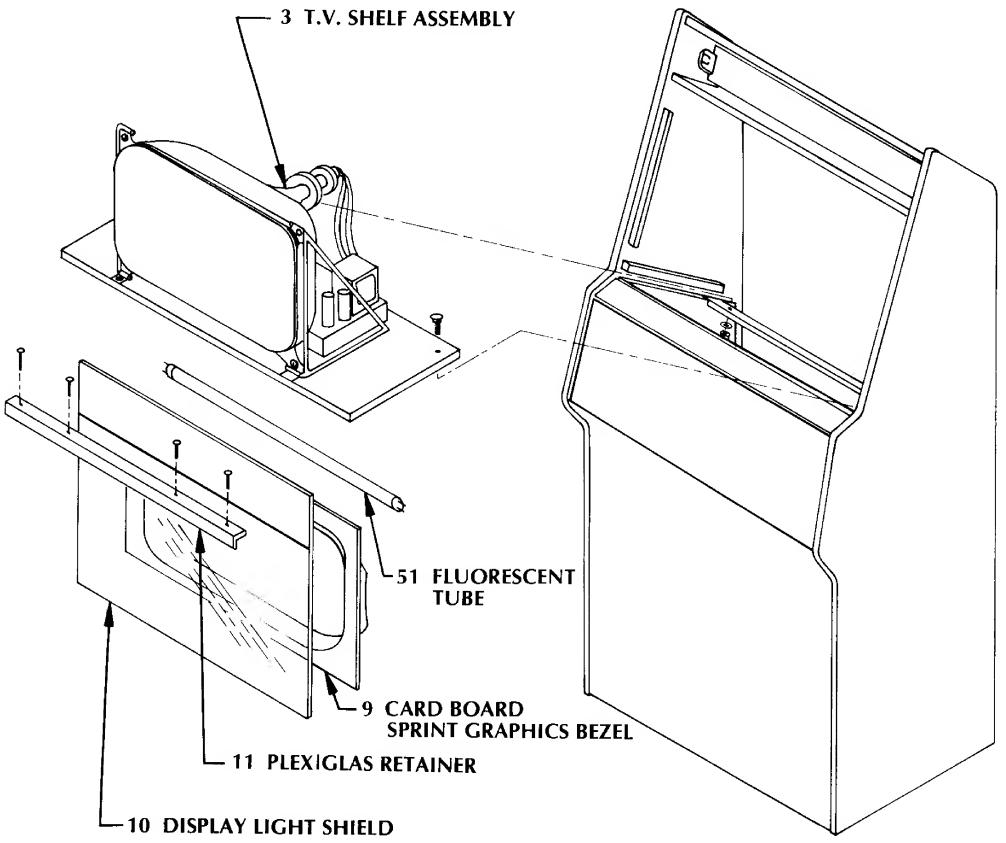
4.5.7 Motor Generator (Top Right of Schematic Sheet 5):

The key to the Motor Generator is the operation of transistor Q1 in conjunction with timer D7,8. Timer D7,8 operates as an oscillator with output frequency dependent upon the resistive charge path of capacitor C22.

Varying the collector to emitter resistive value of transistor Q1, varies the combined resistive charge path of capacitor C22 through transistor Q1 and resistors R21 and R23 in parallel with resistor R22. As the combined resistive value decreases, the output frequency of the timer increases. Variable resistor R23 makes it possible for the technician to adjust the frequency for a desirable motor idle sound.

The conductance of transistor Q1 is varied by grounding any combination of voltage divider resistors R5, R6, R7, and R8. The combinations of these resistors are determined by data, from the microcomputer RAM, applied to the input of Latch D4. Table 4-5 lists the approximate voltages at the base of transistor Q1 (or Q2) for the fifteen different address inputs. These addresses cause a latch condition of Latch D4 only if a low level logic $\overline{\text{MOTOR 1}}$ signal enables Latch D4.

To derive a realistic car motor sound, the output of Timer D7,8 is divided into three separate frequencies by Divider D8, then summed by resistors R42, R43, and R44. A divide by three signal at QB (pin 11) output of D8 is applied to summing resistor R42. Outputs QB and QD (pin 8) are also applied to Exclusive OR Gate C7 to provide a divide by twelve signal at the QA (pin 12) output of D8, which is applied to summing resistor R42.



Indicates same reference number in parts list A006205-01, Section IX

Figure 7-1A Exploded Diagram, Front View

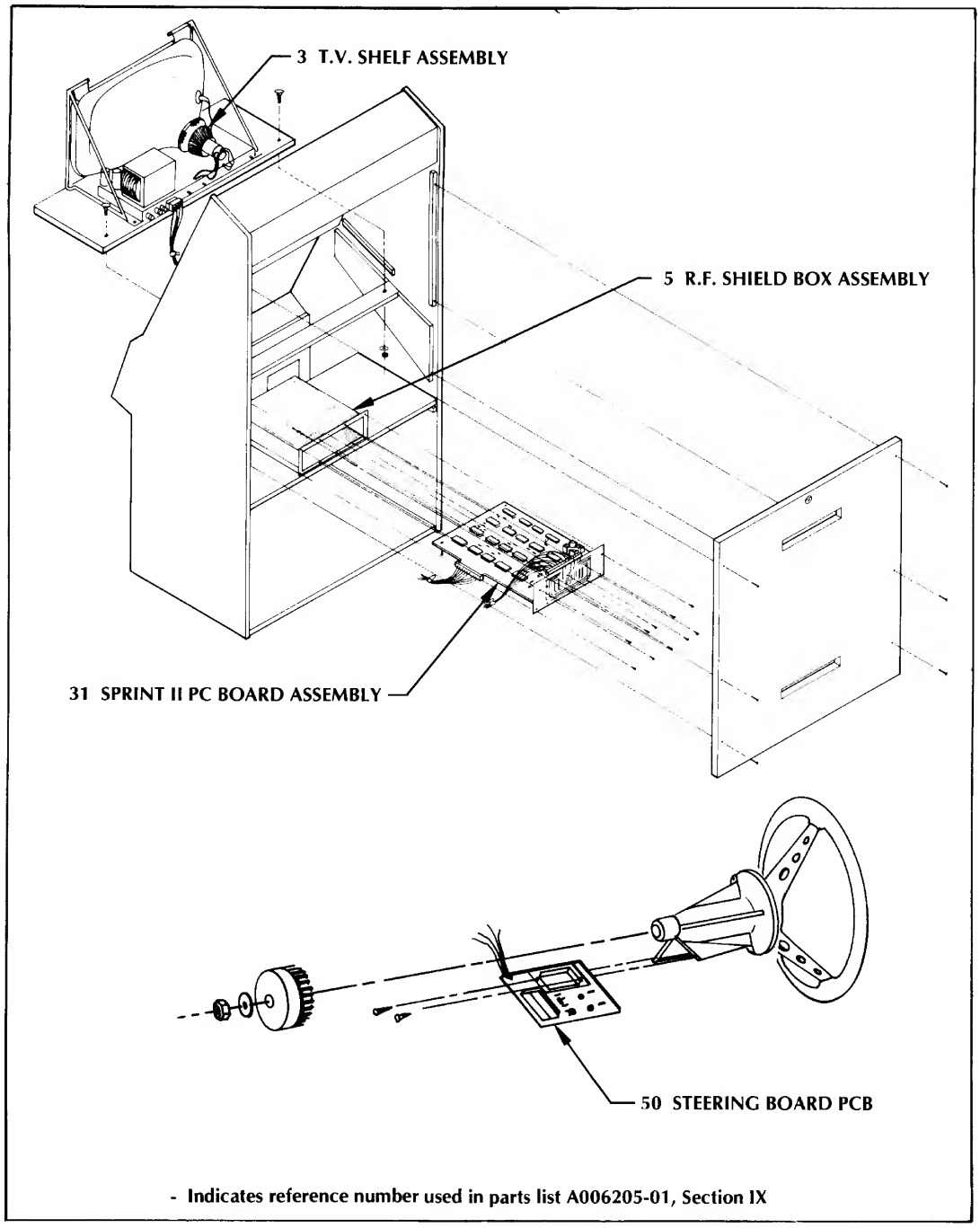
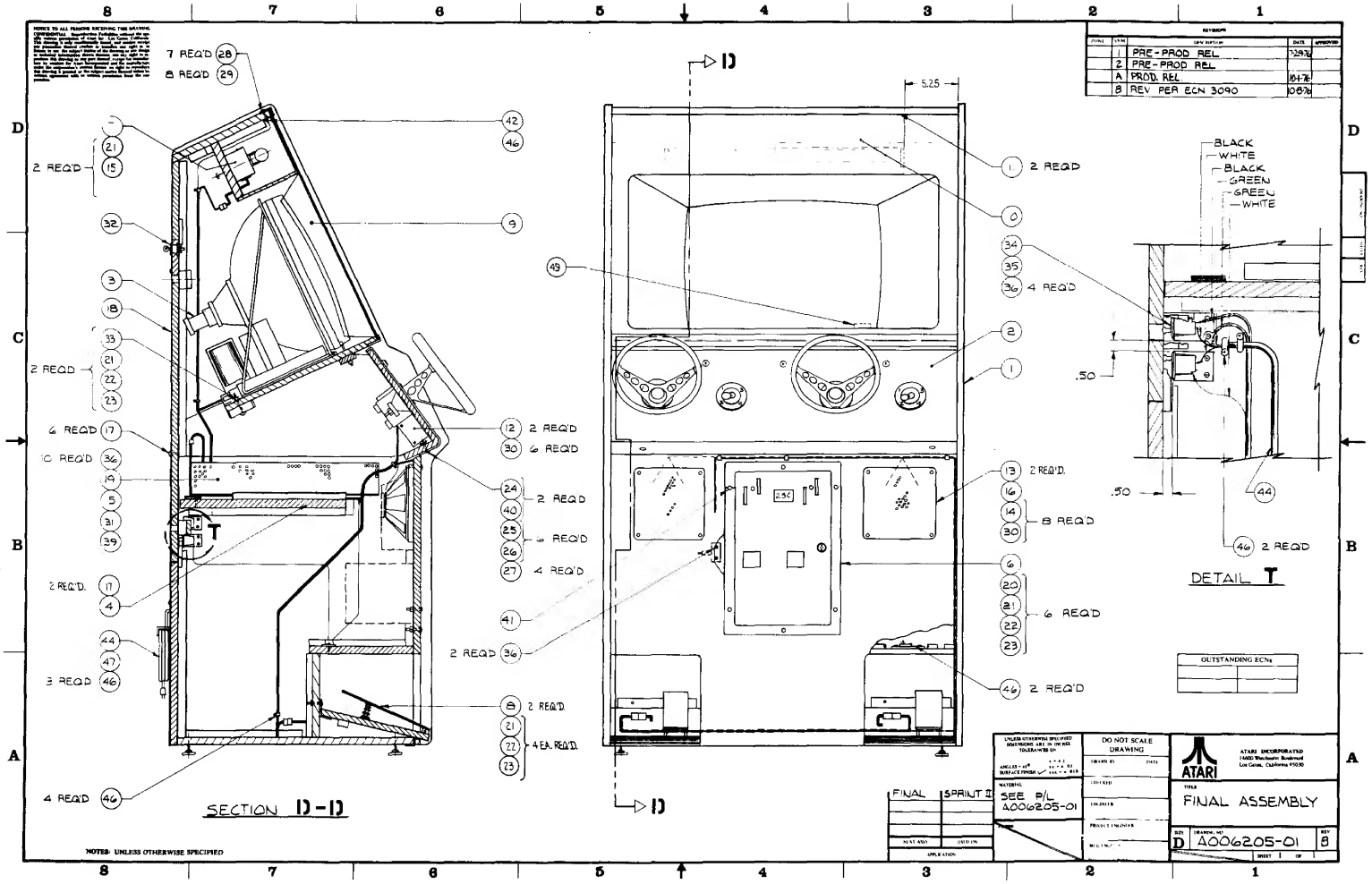


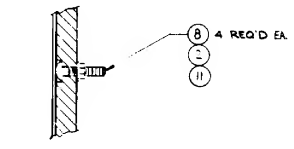
Figure 7-1B Exploded Diagram, Rear View

IX. SCHEMATICS, DRAWINGS, AND PARTS LISTS

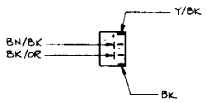
NUMBER	TITLE
A006205-01	Parts List and Drawing Final Assembly
A006206-01	Drawing Control Panel Assembly
A005925	Drawing Electronics Tray Assembly
A006285-01	Parts List and Drawing R.F. Shield Assembly (PCB)
A005922-01	Parts List, Drawing, and Schematic Sprint II PC Board Assembly
A000607	Parts List, Drawing, and Schematic Steering Printed Circuit Assembly
A006278-01	Schematic Harness
(none)	Schematic Motorola Model XM 701-10 TV Monitor


7 REQ'D 28
8 REQ'D 29
2 REQ'D 21 15
32
3 18
2 REQ'D 33 21 22 23
4 REQ'D 17
10 REQ'D 36 19 5 31 39
2 REQ'D. 17 4
44 47
3 REQ'D 46
4 REQ'D 46
42 46
9
12 2 REQ'D
30 6 REQ'D
24 40 2 REQ'D
25 26 6 REQ'D
27 4 REQ'D
41
2 REQ'D 36
8 2 REQ'D.
21 22 23 4 EA. REQ'D.
SECTION D-D
NOTES: UNLESS OTHERWISE SPECIFIED
5.25
49
1 2 REQ'D
0
34 35 36 4 REQ'D
2
1
13 2 REQ'D.
16 14 30 8 REQ'D
6
20 21 22 23 6 REQ'D
46 2 REQ'D
BLACK
WHITE
BLACK
GREEN
GREEN
WHITE
.50
.50
44
46 2 REQ'D
DETAIL T
REVISIONS
1 PRE-PROD REL
2 PRE-PROD REL
A PROD. REL
B REV PER ECN 3090
OUTSTANDING ECNs
DO NOT SCALE DRAWING
FINAL
SPRINT II
SEE P/L A0006205-01
ATARI
ATARI INCORPORATED
1400 Wechester Boulevard
Los Gatos, California 95030
TITLE
FINAL ASSEMBLY
SIZE D
DRAWING NO. A0006205-01
REV B
SHEET 1 OF 1

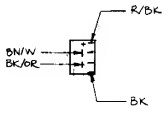
ITEM	QTY	REVISIONS	DATE	APPROVED
	2	PRE-PROD. REL		
	3	PRE-PROD. REL.		
	A	PRODUCTION REL.		
	B	REV PER ECN 3287		



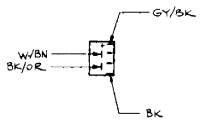
DETAIL J



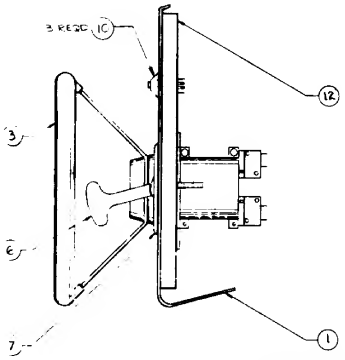
DETAIL L
ONE PLAYER START

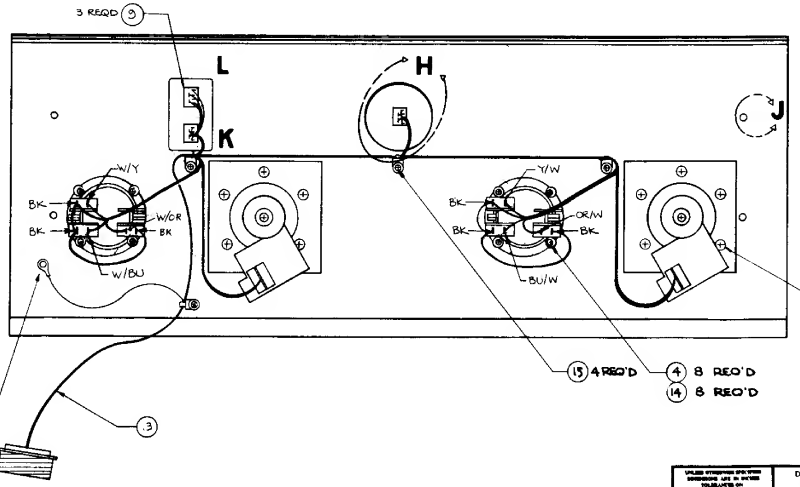


DETAIL H
TRACK SELECT



DETAIL K
TWO PLAYER START





OUTSTANDING ECNs

NOTES: UNLESS OTHERWISE SPECIFIED

DO NOT SCALE DRAWING

ATARI

SEE P/L A006206-01

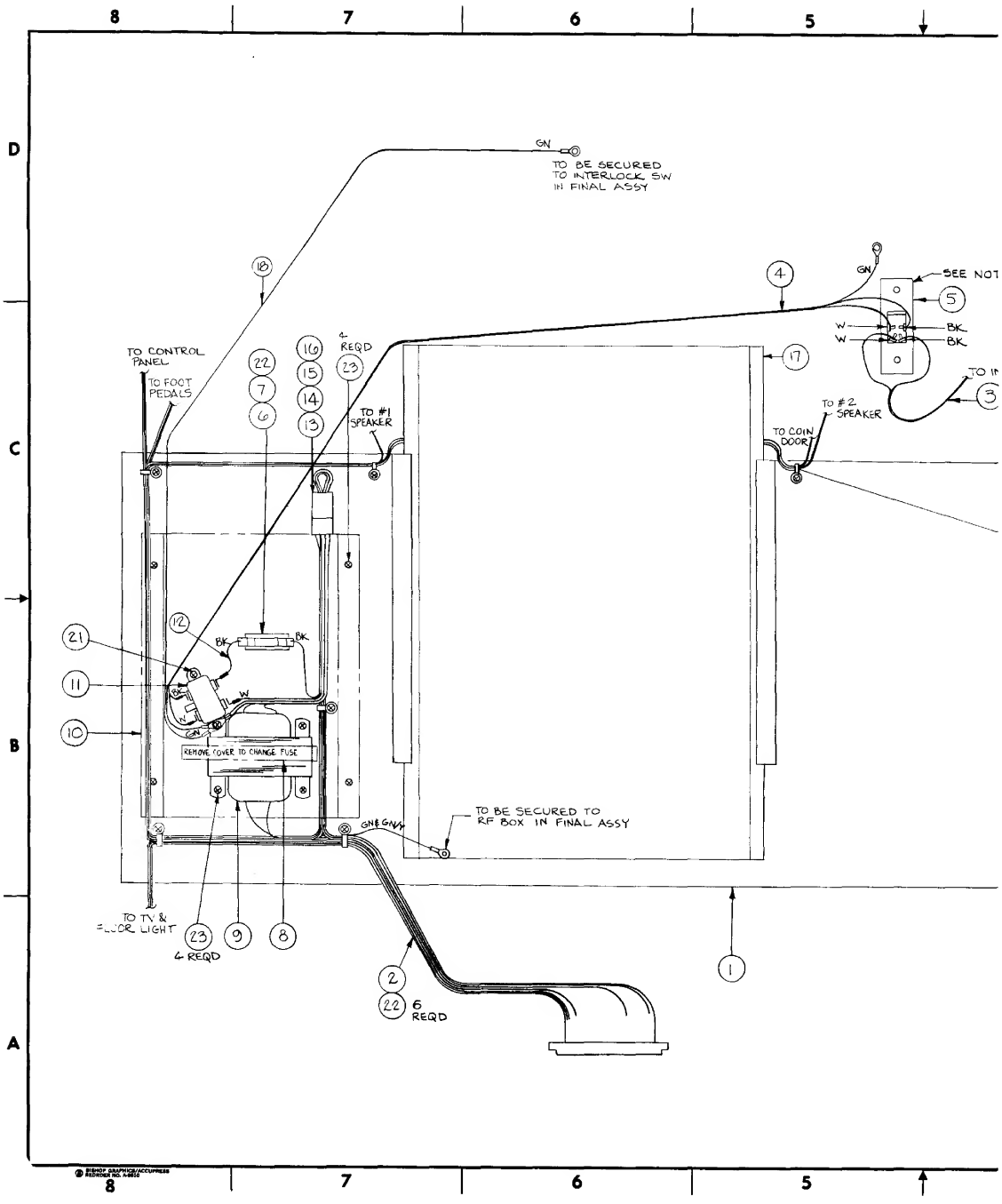
CONTROL PANEL ASS'Y

SIZE D

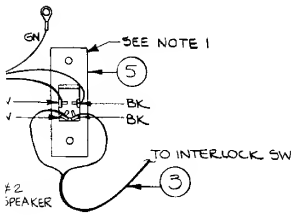
A006206-01

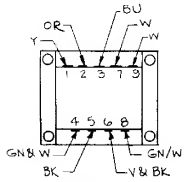
B

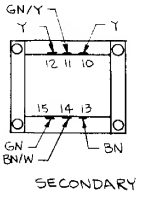
SPRINT 3


8
7
6
5
D
C
B
A
GN
TO BE SECURED TO INTERLOCK SW IN FINAL ASSY
TO CONTROL PANEL
TO FOOT PEDALS
TO #1 SPEAKER
TO #2 SPEAKER
TO COIN DOOR
REQD
SEE NOT
W
BK
REMOVE COVER TO CHANGE FUSE
GN&GN/Y
TO BE SECURED TO RF BOX IN FINAL ASSY
TO TV & FLOOR LIGHT
6 REQD

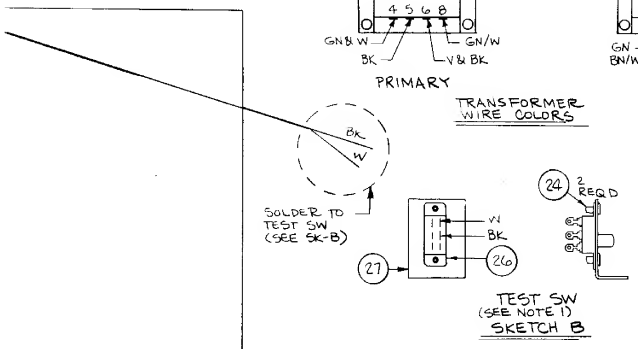
REVISIONS				
ZONE	SYM	DESCRIPTION	DATE	APPROVED
	1	PRE-PROD REL		
	A	PROD REL		
	B	REV PER ECN 3089		







TRANSFORMER WIRE COLORS



OUTSTANDING ECNs	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON:
ANGLES ± 1°
SURFACE FINISH
.x ± .1
.xx ± .03
.xxx ± .010

DO NOT SCALE DRAWING

DRAWN BY DATE

CHECKED

ENGINEER

PROJECT ENGINEER

MATERIAL: SEE P/L

FINISH:

ATARI INCORPORATED
14600 Winchester Boulevard
Los Gatos, California 95030

TITLE: SPRINT II
ELECTRONICS TRAY ASSEMBLY

SIZE	DRAWING NO.	REV
D	A005925-XX	B

SCALE 1:2 SHEET 1 OF 1

NEXT ASSY	USED ON
A005664-01	
	A006205-01
A006205-01	SPRINT II

APPLICATION

ATARI™ Innovative leisure

KEE GAMES a wholly owned subsidiary of Atari, Inc.

ASSEMBLY TITLE / SPRINT II P.C. ASSY.	P/L A005922-01
PARTS LIST SPECIFICATION	Page 1 of 6
Drawn	
Checked	Mech. Eng.
Proj. Eng.	Elec. Eng.
	Mfg. Eng.

Rev. A

Rev.	Description	Date	Apprv.	Rev.	Description	Date	Apprv.
1	PRE PROD.	8/3/76					
A	PRODUCTION REL.	10/1/76					

Item	Part Number	Qty.	Description	
1	005923-01	1	SPRINT P.C. BOARD	
2	10-5101	5	RES., CARBON, 5%, ¼W, 100 OHM	R17,18,35,37,32
3	10-5102	10	" " " " 1K OHM	R1,2,4,19,20,26, 33,38,50,68
4	10-5103	19	" " " " 10K OHM	R3,21,28, ,39-44, 54-61,63,64
5	10-5105	2	" " " " 1M OHM	R6,11
6	10-5182	2	" " " " 1.8K OHM	R48,49
7	10-5222	3	" " " " 2.2K OHM	R15,16,25
8	10-5224	2	" " " " 220K OHM	R8,13
9	10-5225	2	" " " " 2.2M OHM	R5,10
10	10-5331	21	" " " " 330 OHM	R 45,46,51-53, 69-83,86
11	10-5333	2	" " " " 33K OHM	R62,65
12	10-5335	2	" " " " 3.3M OHM	R22,29
13	10-5392	1	" " " " 3.9K OHM	R24
14				
15	10-5474	2	" " " " 470K OHM	R7,12
16	10-5683	2	" " " " 68K OHM	R9,14
17	10-5822	1	" " " " 8.2K OHM	R27
18	19-8D9W2P0	1	RES., WIREWOUND, 20W, 2 OHM	R47
19	19-315502	2	TRIMPOT, 5K OHM	R66,67
20	19-315254	2	TRIMPOT, 250K OHM	R23,R30
21	10-5221	1	RES., CARBON, 5%, ¼W, 220 OHM	R84
22	10-5270	1	" " " " 27 OHM	R85
23				
24				

ASSEMBLY TITLE SPRINT II P.C. ASSY.	P/L A005922-01	REV. A
PARTS LIST SPECIFICATION	Page 2 of 6	

Item	Part Number	Qty.	Description	
25	21-101103	2	CAP., MYLAR, .01uf 100V	C22,23
26				
27				
28	24-160808	2	CAP., ELECTROLYTIC, 8000uf, 16V	C65,66
29	24-25016	4	" " 10uf, 25V	C17,18,24,25
30	24-250108	2	" " 1000uf, 25V	C49,50
31	24-250227	1	" " 220uf, 25V	C12
32	24-250478	1	" " 4700uf, 25V	C67
33				
34				
35	27-250102	2	CAP., CERAMIC DISC, .001uf, 25V	C55,62
36	27-250103	8	" " " .01uf, 25V	C28,30,57,64, 44-47
37	27-250104	42	" " " .1uf, 25V	C1-4,13-16,19-21, 26,27,29,31-36, 41-43,48,51,52, 54,56,58,59,61, 63,68,69,6-11, 39,70
38				
39				
40	28-101101	2	CAP., DIPPED MICA, 100pf, 100V	C37,38
41	28-101221	2	" " " 220pf, 100V	C53,60
42				
43				
44				
45				
46	31-A14F	2	DIODE, A14,F	CR6,7
47	31-MR501	2	" MR501	CR4,5
48	31-IN914	3	" IN914	CR1,2,3
49				
50				
51	33-2N3644	2	TRANSISTOR, 2N3644	Q1,Q2
52				
53				
54				
55				
56				
57	37-7400	2	INTEGRATED CIRCUIT, 7400	F8,D0

ASSEMBLY TITLE SPRINT II P.C. ASSY. P/L A005922-01 REV. A

PARTS LIST SPECIFICATION

Item	Part Number	Qty.	Description			
58	37-7402	1	INTEGRATED CIRCUIT,		7402	P2
59	37-7404	6	"	"	7404	E3,E4,H5,J5,L6,N9
60	37-7408	5	"	"	7408	B2,C2,N3,C5,A6
61	37-7410	1	"	"	7410	R7
62	37-7414	2	"	"	7414	A5,L9
63	37-7420	1	"	"	7420	A8
64	37-7430	1	"	"	7430	N4
65	37-7432	5	"	"	7432	A2,L2,P3,F6,J8
66	37-7437	1	"	"	7437	R9
67	37-7474	3	"	"	7474	R1,L8,M9
68	37-74S74	1	"	"	74S74	R8
69	37-7475	3	"	"	7475	B4,C4,D4
70	37-7483	2	"	"	7483	L4,M4
71	37-7486	1	"	"	7486	C7
72	37-7490	1	"	"	7490	C6/7
73	37-7492	2	"	"	7492	B8,D8
74	37-9312	2	"	"	9312	F9,H9
75	37-74153	1	"	"	74153	M8
76	37-74156	1	"	"	74156	J9
77	37-74LS163	8	"	"	74LS163	M5,N5,P5,R5, M6,N6,P6,R6
78	37-74164	2	"	"	74164	B7,D7
79	37-74165	8	"	"	74165	E7,F7,H7,J7, K7,L7,M7,N7
80	37-74166	1	"	"	74166	R3
81	37-74174	3	"	"	74174	F5,L5,A7
82	37-74175	1	"	"	74175	N2
83	37-74279	1	"	"	74279	H6
84	37-9301	5	"	"	9301	D2,F2,P7,E8,K8
85	37-9316	5	"	"	9316	R2,L3,M3,N8,P8
86	37-9322	3	"	"	9322	H2,J2,K2
87	37-9334	1	"	"	9334	H8
88	37-555	2	"	"	555	B7/8,D7/8
89	37-74367	3	"	"	74367	E5,K5,E6
90	37-21L02A	8	"	"	21L02A	F3,H3,J3,K3, F4,H4,J4,K4
91	37-LM323	1	REGULATOR		LM323	
92	37-TDA1004	2	OP-AMP		TDA1004	B9,D9

ASSEMBLY TITLE		P/L A005922	REV.
PARTS LIST SPECIFICATION			Page 4 of 6
Item	Part Number	Qty.	Description
93			
94			
95			
96			
97	62-001	1	SWITCH, SPST, MOMENTARY SW3
98	66-114P1T	1	SWITCH, SPST, x4, DIP SW2
99	66-118P1T	1	SWITCH, SPST, x8, DIP SW1
100			
101			
102			
103	72-1608C	2	SCREWS, PAN HD., PHIL., 6-32 x ½ LG, CRES
104	75-016	2	WASHER, FLAT #6
105	75-056	2	WASHER, LOCK, INT STAR, #6
106	75-916C	2	NUT, HEX, #6-32 CRES
107			
108			
109	78-06001	1	HEATSINK, (LM323)
110	78-06009	2	HEATSINK, (TDA1004)
111	78-13016	A/R	CEMENT, (TDA1004 HEATSINK)
112	78-16005	1	SILPAD (LM323)
113			
114			
115			
116			
117A	79-42518	16	SOCKET 18 PIN, LOW INSERTION FO,HQ,JO,KO,LO,MO, (USED ON -01 BOARDS ONLY) NO,PO,F1,H1,J1,K1, L1,M1,N1,P1
117B	79-42518	8	SOCKET 18 PIN, LOW INSERTION LO,L1,MO,M1,NO,N1, (USED ON -02 BOARDS ONLY) PO,P1
117C			NOT USED ON -03 BOARDS
118A			NOT USED ON -01 BOARDS
118B	79-42524	2	SOCKET, 24 PIN, LOW INSERTION AO,CO (USED ON -02 BOARDS ONLY)
118C	79-42524	4	SOCKET, 24 PIN, LOW INSERTION AO,DO,EO (USED ON -03 BOARDS ONLY)

Item	Part Number	Qty.	Description		
119	79-42540	1	SOCKET, 40 PIN, LOW INSERTION	C3	
120					
121					
122					
123	90-102	1	CRYSTAL, 12.096MHZ	Y1	
124					
125					
126					
127	006380-01	1	SPRINT II PROGRAM PROM 1	L1	
			(NOT USED ON -03 BOARDS)		
128	006381-01	1	SPRINT II PROGRAM PROM 2	L0	NOT USED ON -03 BOARDS
129	006382-01	1	" " " " 3	M1	
130	006383-01	1	" " " " 4	M0	
131	006384-01	1	" " " " 5	N1	
132	006385-01	1	" " " " 6	N0	
133	006386-01	1	" " " " 7	P1	
134	006387-01	1	" " " " 8	P0	
135					
136					
137	006388-01	1	SPRINT II RACE TRACK PROM 1	F1	USED ON -01 BOARDS ONLY
138	006389-01	1	" " " " " 2	F0	
139	006390-01	1	" " " " " 3	H1	
140	006391-01	1	" " " " " 4	H0	
141	006392-01	1	" " " " " 5	J1	
142	006393-01	1	" " " " " 6	J0	
143	006394-01	1	" " " " " 7	K1	
144	006395-01	1	" " " " " 8	K0	
145					
146					
147	006396-01	1	SPRINT II CHARACTER PROM LSB	P4	
148	006397-01	1	" " " " MSB	R4	
149					
150					
151	006398-01	1	SPRINT II RACE CAR PROM LSB	K6	
152	006399-01	1	" " " " " MSB	J6	
153					
154					

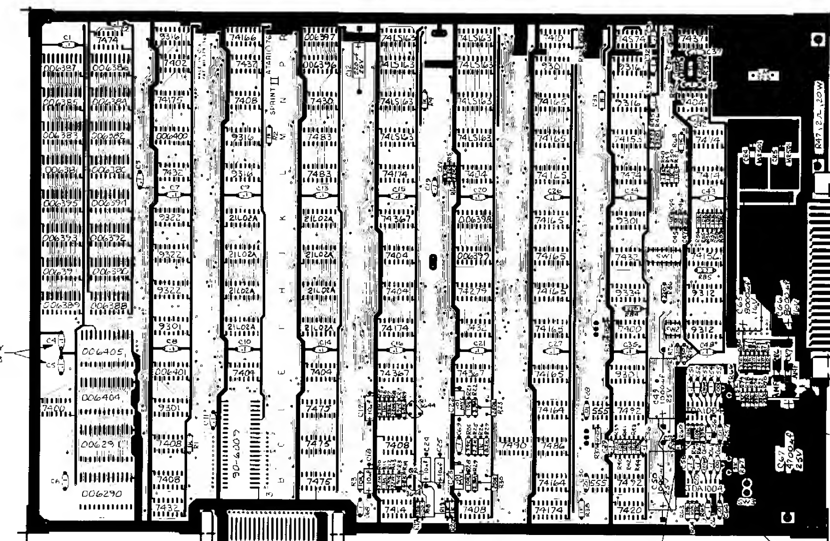
ASSEMBLY TITLE	P/L A005922	REV.

PARTS LIST SPECIFICATION

Item	Part Number	Qty.	Description
155	006400-01	1	SPRINT II SYNC PROM M2
156			
157			
158	006401-01	1	SPRINT II ADDRESS DECODE PROM
159			
160			
161			
162			
163	006404-01	1	SPRINT II PROGRAM ROM 1 D1
			(USED ON -03 BOARDS ONLY)
164	006405-01	1	SPRINT II PROGRAM ROM 2 E1
			(USED ON -03 BOARDS ONLY)
165			
166			
167	006290-01	1	SPRINT II RACE TRACK ROM 1 A1
			(USED ON -02 AND -03 BOARDS ONLY)
168	006291-01	1	SPRINT II RACE TRACK ROM 2 C1
			(USED ON -02 AND -03 BOARDS ONLY)
169	90-6009	1	INTEGRATED CIRCUIT C3

ZONE	SYM	DESCRIPTION	DATE	APPROVED
	A	PRODUCTION RELEASE		

NOTICE TO ALL PERSONS RECEIVING THIS DRAWING



CAP C4 FOR -01 ONLY
CAP C5 FOR -02 -03 ONLY

SEE MOD. 1

SEE NOTE 2

NOTES:

1. THIS ASSEMBLY TO BE USED 005923 REV 'B' BOARDS.
2. ITEMS 110 (HEATSINK) TO BE CEMENTED TO ITEM 92 (TDA 1004) WITH HEATSINK CEMENT ITEM 111

MODIFICATIONS:

1. ADD A .1µf CAP(C70) BETWEEN +30V PLANE AND GROUND AS SHOWN.

DWG NO / VERSION	006380	006381	006382	006383	006384	006385	006386	006387	006388	006389	006390	006391	006392	006393	006394	006395	006404	006405	006290	006291
-01	L1	L0	M1	M0	N1	N0	P1	P0	F1	F0	H1	H0	J1	J0	K1	K0				
-02	L1	L0	M1	M0	N1	N0	P1	P0											B1	C1
-03																	D1	E1	B1	C1

OUTSTANDING ECN's

NEXT ASSY	USED ON
A006205-01	SPRINT II

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL: SEE PL A005922 -01, -02, -03

DO NOT SCALE DRAWING

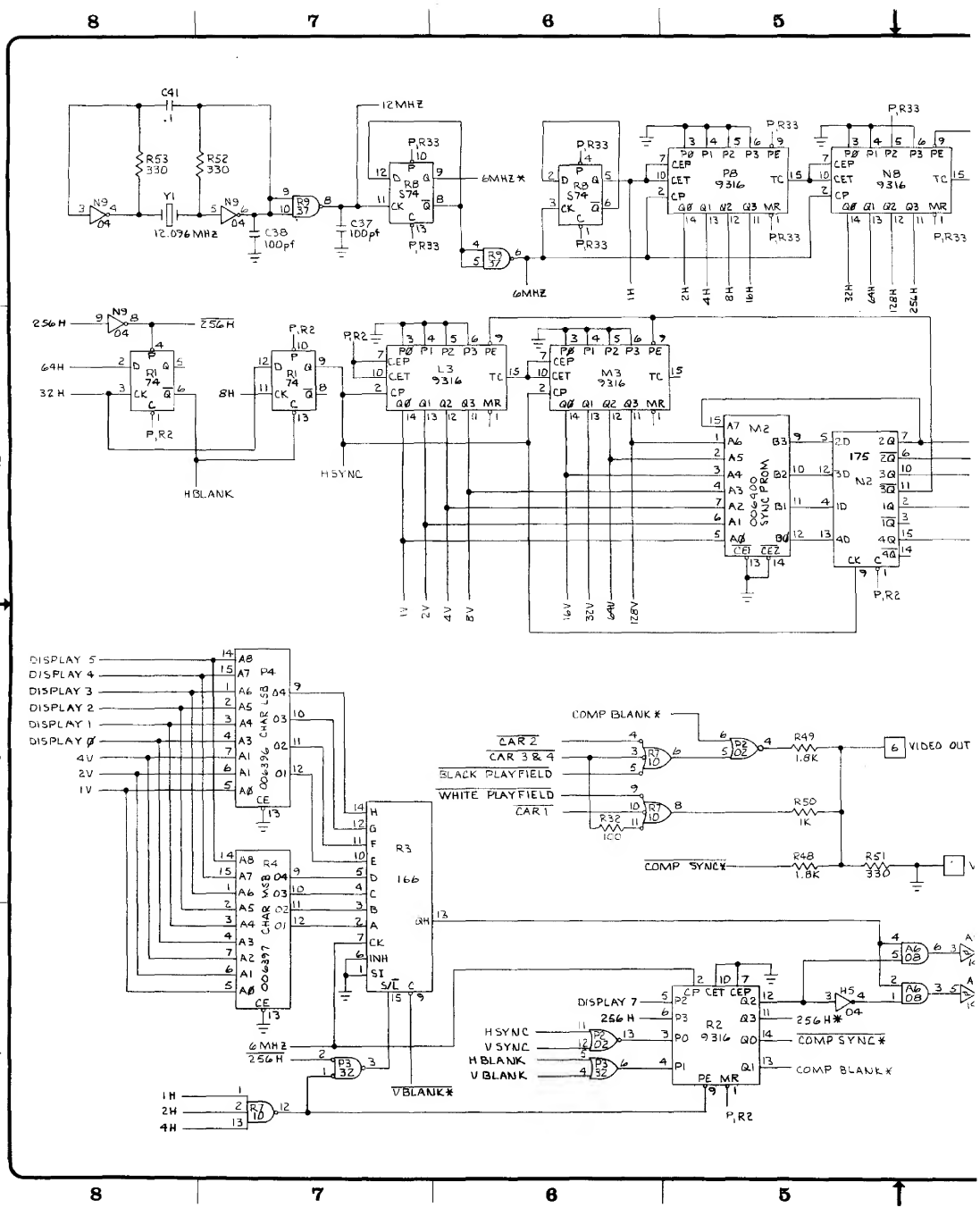
ATARI INCORPORATED
14600 Winchester Boulevard
Los Gatos, California 95030

TITLE: ASSEMBLY, SPRINT II P.C. BD

SIZE: D | DRAWING NO: A005922-XX | REV: A

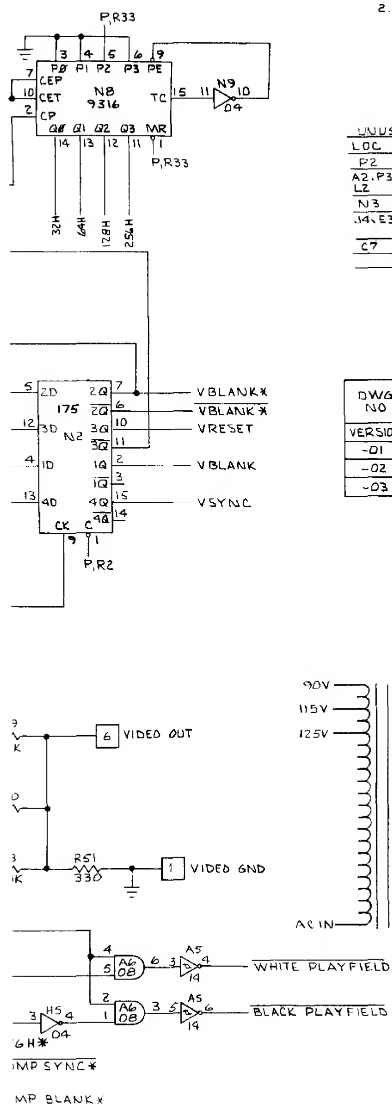
SCALE: 1/1 | SHEET 1 OF 1

NOTES: UNLESS OTHERWISE SPECIFIED


8
7
6
5
D
C
B
A
C41
.1
R53
330
R52
330
Y1
12.096 MHZ
C38
100pf
C37
100pf
12MHZ
6MHZ*
6MHZ
P,R33
P,R2
256H
64H
32H
8H
HBLANK
HSYNC
1H
2H
4H
8H
16H
32H
64H
128H
256H
1V
2V
4V
8V
16V
32V
64V
128V
M2
M3
N2
006400
SYNC PROM
DISPLAY 5
DISPLAY 4
DISPLAY 3
DISPLAY 2
DISPLAY 1
DISPLAY 0
CHAR LSB
CHAR MSB
006396
006397
R3
166
R4
VBLANK*
CAR 2
CAR 3 & 4
BLACK PLAYFIELD
WHITE PLAYFIELD
CAR 1
COMP BLANK*
COMP SYNC*
R49
1.8K
R50
1K
R48
1.8K
R51
330
VIDEO OUT
DISPLAY 7
256H
HSYNC
VSYNC
HBLANK
VBLANK
R2
9316
PE MR
COMP SYNC*
COMP BLANK*

NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTANCE VALUES ARE IN OHMS.
2. CAPACITANCE VALUES ARE IN MICROFARADS.

REVISIONS				
SYM	DESCRIPTION	INITIALS and DATE: DRFTG	CHECK	ENGRG
1	PRE-PROD. RELEASE			
A	PRODUCTION RELEASE			

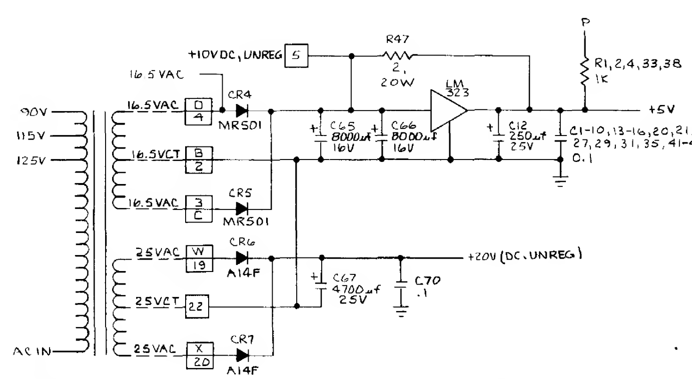


UNUSED GATES	
LOC	TYPE
P2	02
A2, P3, L2	32
N3	08
J4, E3,	04
C7	86

REF DESIGNATION	
HIGHEST	NOT USED
R85	R34,36,31
C69	C40
CR7	
Q2	
SW3	
Y1	

REFERENCE ONLY

DWG NO / VERSION	006380	006381	006382	006383	006384	006385	006386	006387	006388	006389	006390	006391	006392	006393	006394	006395				006404	006405	006290	006291
-01	L1	L0	M1	M0	N1	N0	P1	P0	F1	F0	H1	H0	J1	J0	K1	K0							
-02	L1	L0	M1	M0	N1	N0	P1	P0														B1	C1
-03																				D1	E1	B1	C1



SYNC, PLAYFIELD AND POWER CIRCUIT

A005922	SPRINT 2
NEXT ASSY	USED ON
APPLICATION	

INTERPRET THIS DRAWING PER USASI Y14.5

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON
FRACTIONS = ±1/16 .x = ±.1
ANGLES = ±1° .xx = ±.03
SURFACE FINISH ✓ .xxx = ±.010

MATERIAL:

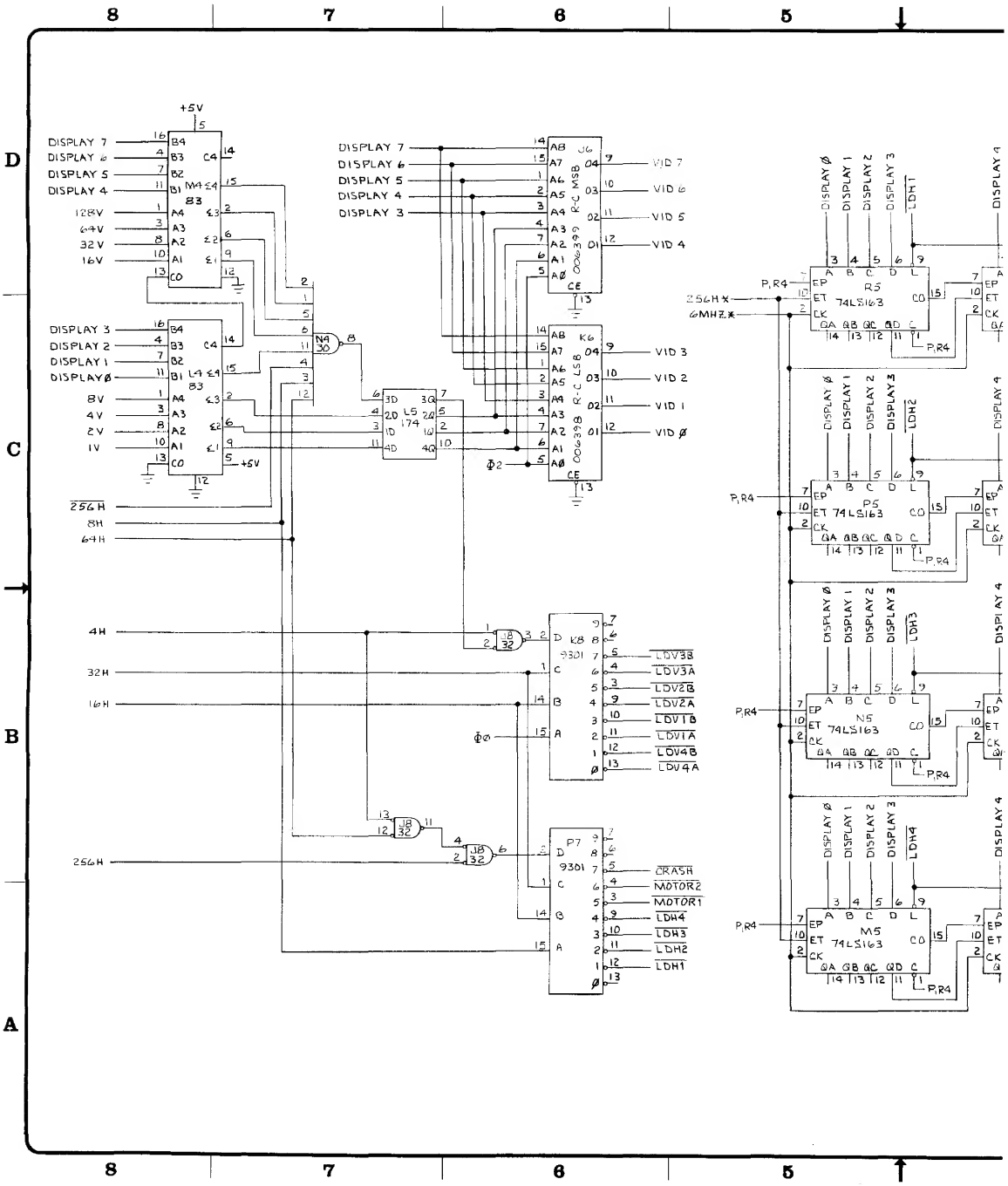
DRAWN BY — DATE
CHECKED
DESIGN ENGINEER
PROJECT ENGINEER
DOCUMENT CONTROL
APPROVED —

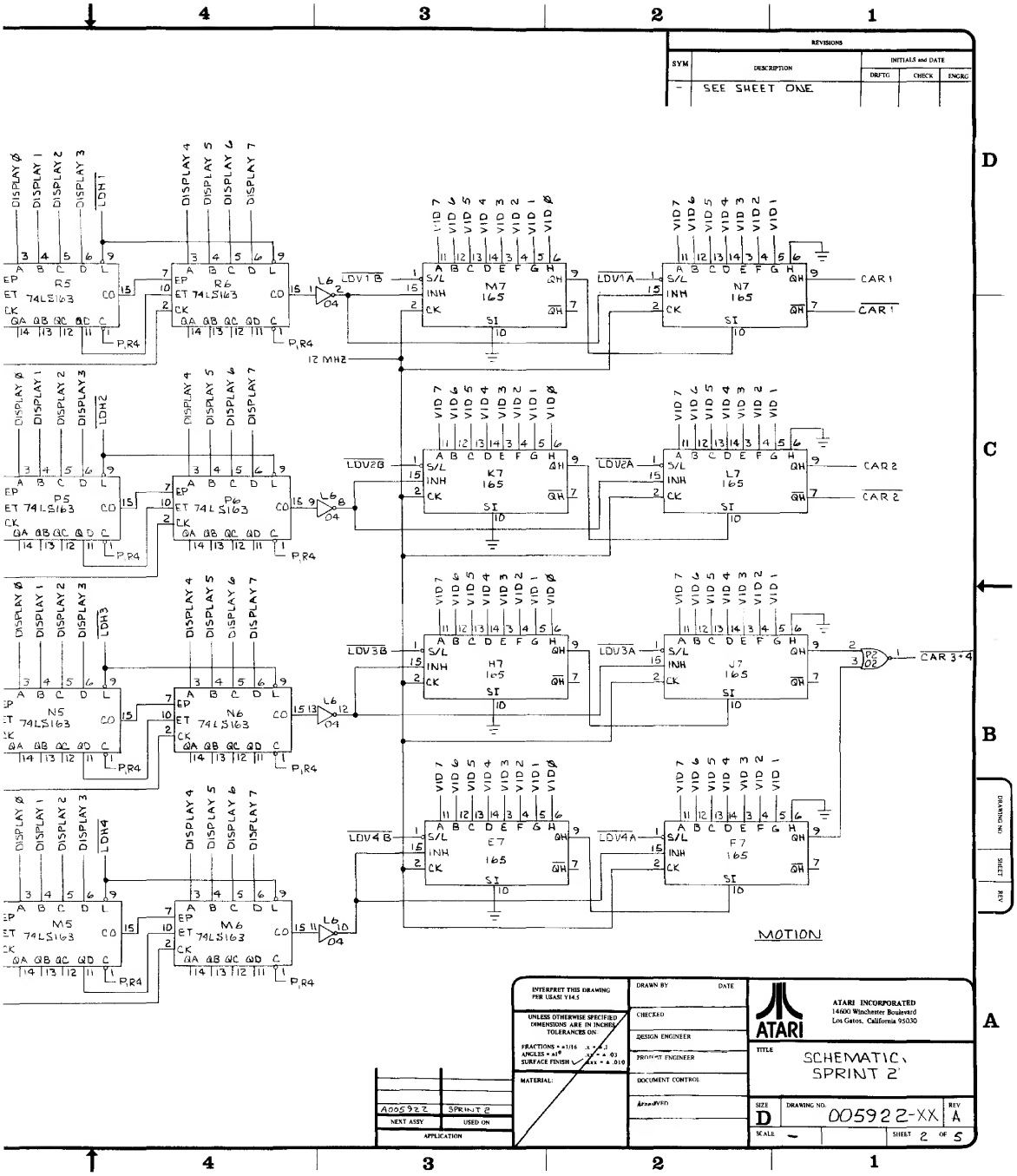
ATARI INCORPORATED
14600 Winchester Boulevard
Los Gatos, California 95030

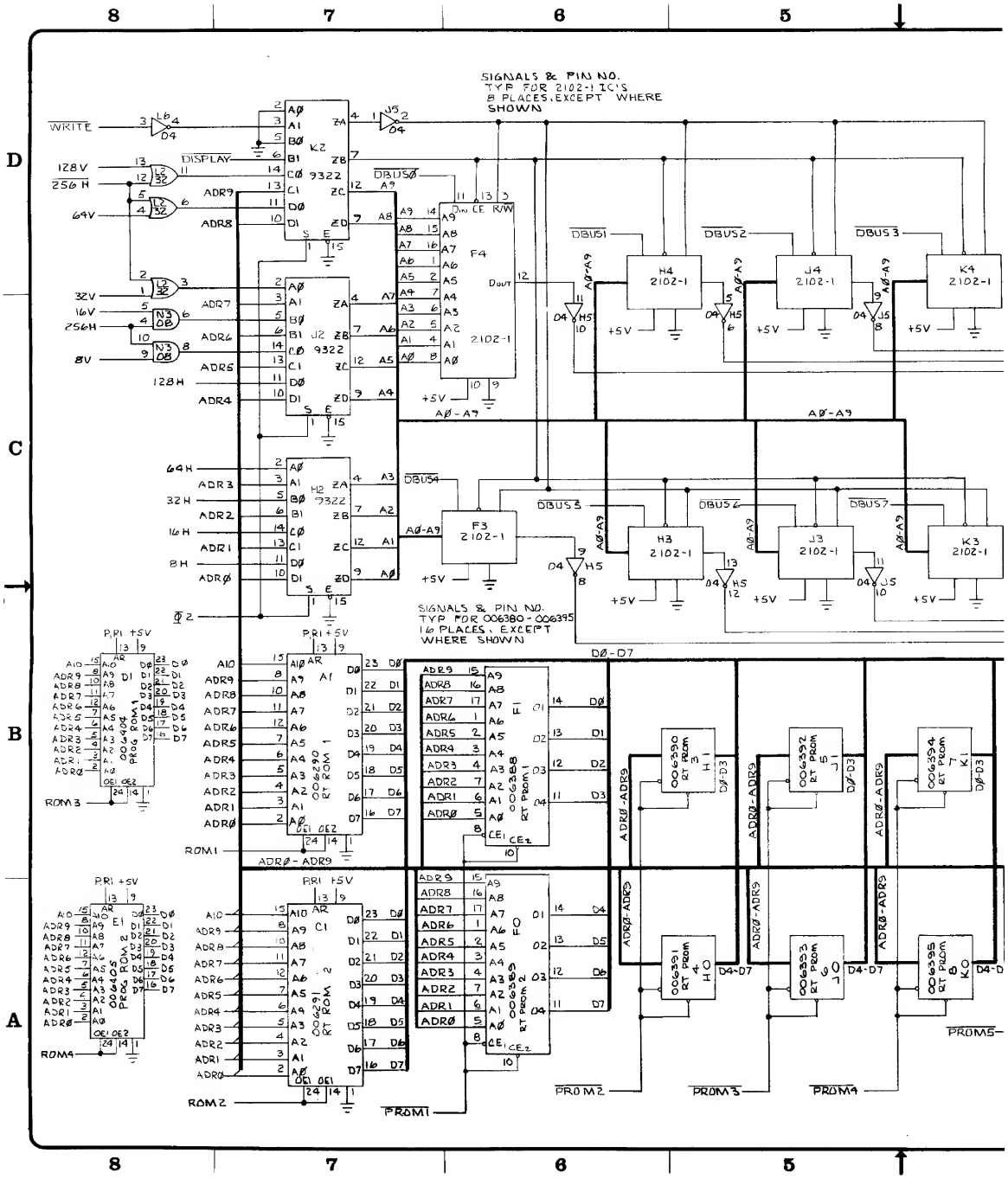
TITLE: SCHEMATIC, SPRINT 2

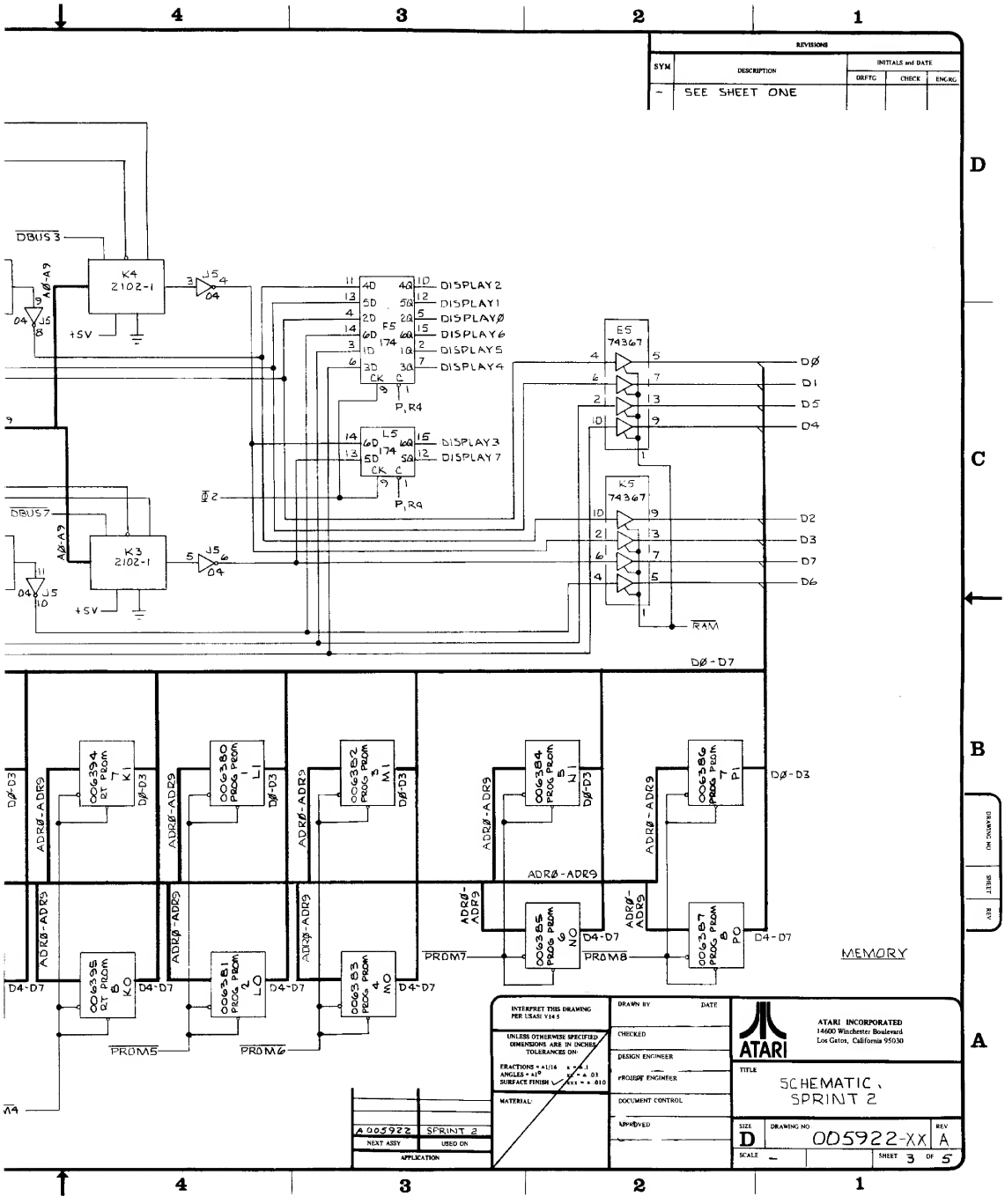
SIZE: D | DRAWING NO: 005922-XX | REV: A

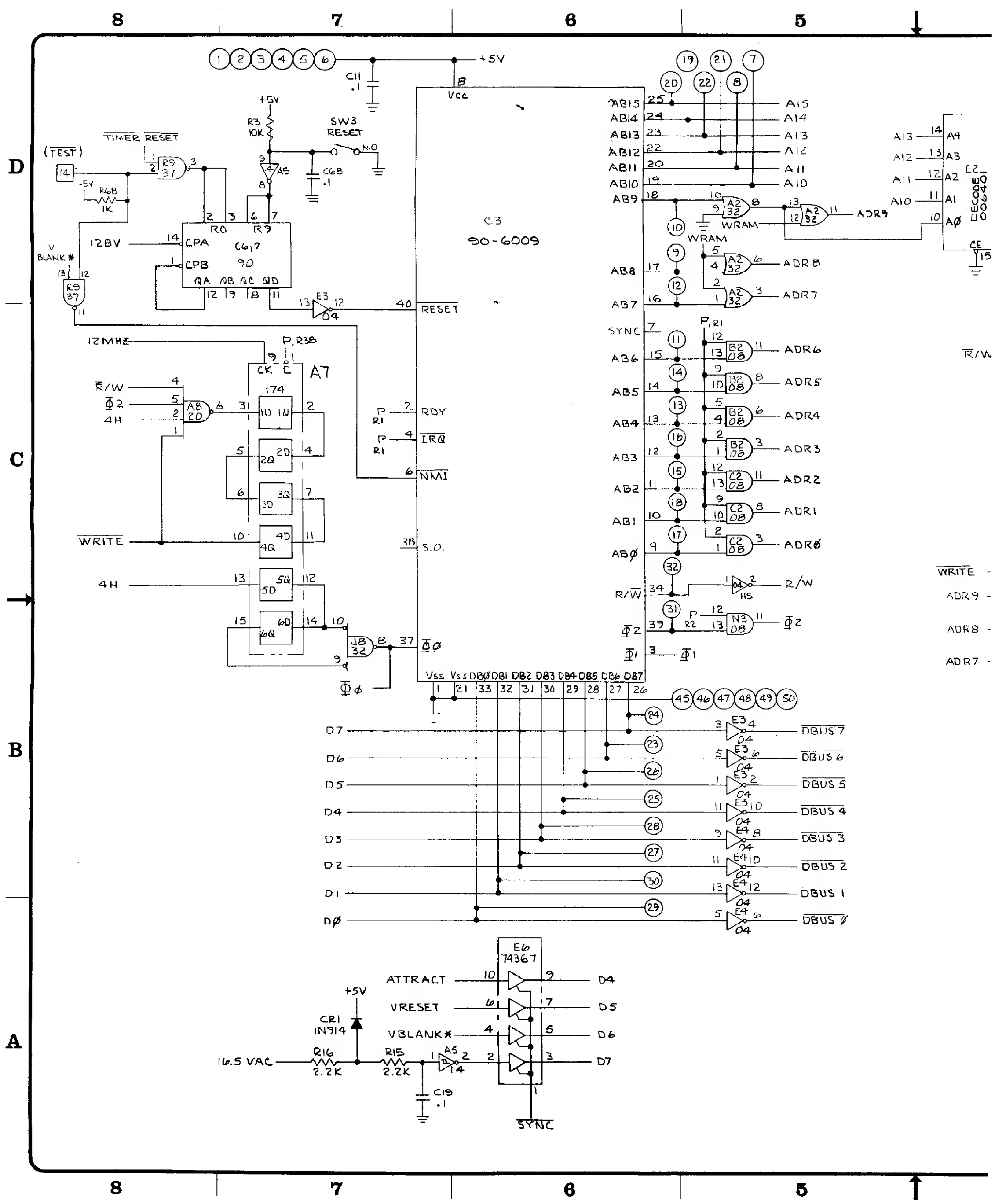
SCALE — | SHEET 1 OF 5


8
7
6
5
D
C
B
A
+5V
DISPLAY 7
DISPLAY 6
DISPLAY 5
DISPLAY 4
128V
64V
32V
16V
DISPLAY 3
DISPLAY 2
DISPLAY 1
DISPLAYØ
8V
4V
2V
1V
256H
8H
64H
4H
32H
16H
256H
ΦØ
Φ2
VID 7
VID 6
VID 5
VID 4
VID 3
VID 2
VID 1
VID Ø
LDV3B
LDV3A
LDV2B
LDV2A
LDV1B
LDV1A
LDV4B
LDV4A
CRASH
MOTOR2
MOTOR1
LDH4
LDH3
LDH2
LDH1
P,R4
256HX
6MHZX
74LS163
74LS174
9301
R-C MSB 006399
R-C LSB 006398

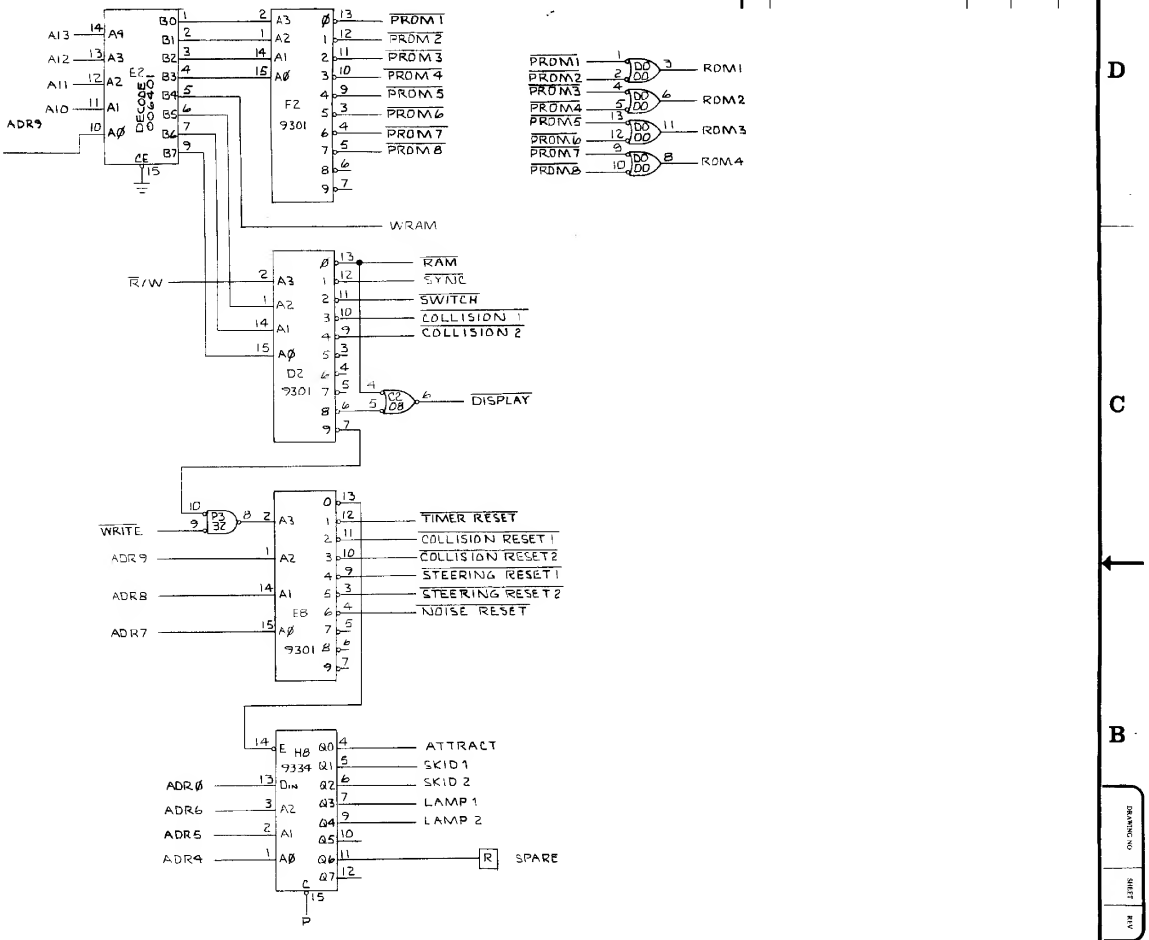

REVISIONS
SYM
DESCRIPTION
INITIALS and DATE
DRFTG
CHECK
ENGRG
SEE SHEET ONE
DISPLAY Ø
DISPLAY 1
DISPLAY 2
DISPLAY 3
LDH1
DISPLAY 4
DISPLAY 5
DISPLAY 6
DISPLAY 7
LDH2
LDH3
LDH4
R5
R6
M5
M6
N5
N6
P5
P6
74LS163
P,R4
12 MHZ
LDV1B
LDV1A
LDV2B
LDV2A
LDV3B
LDV3A
LDV4B
LDV4A
M7
N7
K7
L7
H7
J7
E7
F7
165
VID 7
VID 6
VID 5
VID 4
VID 3
VID 2
VID 1
VID Ø
CAR 1
CAR 2
CAR 3·4
MOTION
ATARI INCORPORATED
14600 Winchester Boulevard
Los Gatos, California 95030
ATARI
TITLE
SCHEMATIC, SPRINT 2
DRAWN BY
DATE
CHECKED
DESIGN ENGINEER
PRODUCT ENGINEER
DOCUMENT CONTROL
Approved
MATERIAL:
A005922
SPRINT 2
NEXT ASSY
USED ON
APPLICATION
SIZE
D
DRAWING NO.
005922-XX
REV
A
SCALE
SHEET 2 OF 5
DRAWING NO.
SHEET
REV


SIGNALS & PIN NO.
TYP FOR 2102-1 IC'S
8 PLACES, EXCEPT WHERE
SHOWN
WRITE
DISPLAY
128V
256H
64V
32V
16V
8V
128H
64H
32H
16H
8H
ADR9
ADR8
ADR7
ADR6
ADR5
ADR4
ADR3
ADR2
ADR1
ADRØ
DBUSØ
DBUS1
DBUS2
DBUS3
DBUS4
DBUS5
DBUS6
DBUS7
AØ-A9
DØ-D7
F4
F3
H4
J4
K4
H3
J3
K3
2102-1
+5V
ROM1
ROM2
ROM3
ROM4
PROM1
PROM2
PROM3
PROM4
PROM5
SIGNALS & PIN NO.
TYP FOR 006380-006395
16 PLACES, EXCEPT
WHERE SHOWN
ADRØ-ADR9
D4-D7
D4-D3
8
7
6
5
D
C
B
A


REVISIONS
SYM
DESCRIPTION
INITIALS and DATE
DRFTG
CHECK
ENG.RG
~
SEE SHEET ONE
DBUS3
DBUS7
K4 2102-1
K3 2102-1
A0-A9
+5V
J5 04
J6 04
DISPLAY2
DISPLAY1
DISPLAY0
DISPLAY6
DISPLAY5
DISPLAY4
DISPLAY3
DISPLAY7
F5 74174
L5 74174
P1R4
P1R9
E5 74367
K5 74367
D0
D1
D5
D4
D2
D3
D7
D6
RAM
D0-D7
006394 QT PROM K1
006380 PROG PROM L1
006382 PROG PROM M1
006384 PROG PROM N1
006386 PROG PROM P1
006395 QT PROM K0
006381 PROG PROM L0
006383 PROG PROM M0
006385 PROG PROM N0
006387 PROG PROM P0
ADR0-ADR9
D0-D3
D4-D7
PROM5
PROM6
PROM7
PROM8
MEMORY
INTERPRET THIS DRAWING PER USAS Y14.5
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON:
FRACTIONS ± 1/16 .x ± .1 .xx ± .03
ANGLES ± 1°
SURFACE FINISH .xxx ± .010
MATERIAL:
DRAWN BY
DATE
CHECKED
DESIGN ENGINEER
PROJECT ENGINEER
DOCUMENT CONTROL
APPROVED
ATARI
ATARI INCORPORATED
14600 Winchester Boulevard
Los Gatos, California 95030
TITLE
SCHEMATIC, SPRINT 2
A 005922
SPRINT 2
NEXT ASSY
USED ON
APPLICATION
SIZE
D
DRAWING NO
005922-XX
REV
A
SCALE
SHEET 3 OF 5
DRAWING NO
SHEET
REV



+5V
C11 .1
(TEST)
TIMER RESET
R29 37
+5V
R48 1K
R3 10K
SW3 RESET
N.O.
A5
C68 .1
RO
R9
CPA
CPB
C6,7 90
QA QB QC QD
128V
V BLANK*
R9 37
E3 04
RESET
12MHZ
P, R38
CK C
A7
174
R/W
Φ2
4H
A8 20
WRITE
4H
J8 32
Φ0
RDY
IRQ
NMI
S.O.
C3
90-6009
Vcc
AB15 AB14 AB13 AB12 AB11 AB10 AB9 AB8 AB7 SYNC AB6 AB5 AB4 AB3 AB2 AB1 AB0
A15 A14 A13 A12 A11 A10
A2 32
WRAM
ADR9 ADR8 ADR7 ADR6 ADR5 ADR4 ADR3 ADR2 ADR1 ADR0
B2 08
C2 08
R/W
H5
N3 08
Φ2
Φ1
Vss Vss DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
D7 D6 D5 D4 D3 D2 D1 D0
E3 04
E4 04
DBUS 7 DBUS 6 DBUS 5 DBUS 4 DBUS 3 DBUS 2 DBUS 1 DBUS 0
E6 74367
ATTRACT
VRESET
VBLANK*
+5V
CR1 1N914
16.5 VAC
R16 2.2K
R15 2.2K
C19 .1
SYNC
D4 D5 D6 D7
A13 A12 A11 A10
A4 A3 A2 A1 A0
E2
DECODE
CE
WRITE
ADR9
ADR8
ADR7



MICROPROCESSOR

REVISIONS				
SYM	DESCRIPTION	INITIALS and DATE: DRFTG	CHECK	ENG.RG
-	SEE SHEET ONE			

INTERPRET THIS DRAWING PER USASI Y14.5

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS = ±1/16 ANGLES = ±1° SURFACE FINISH = x.xx = ±.03 xxx = ±.010

MATERIAL

DRAWN BY DATE

CHECKED

DESIGN ENGINEER

PROJECT ENGINEER

DOCUMENT CONTROL

APPROVED

A005922 | SPRINT 2

NEXT ASSY | USED ON

APPLICATION

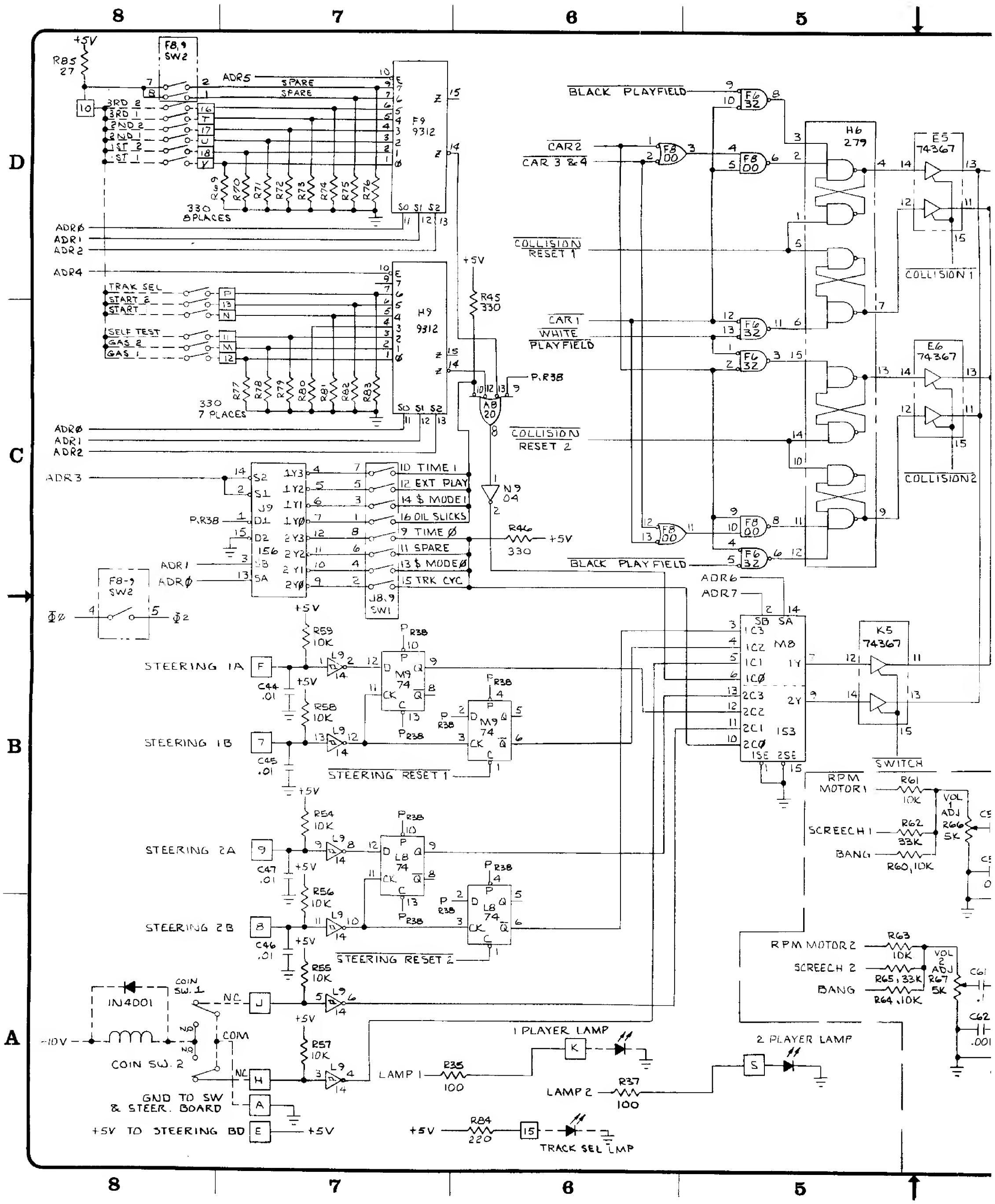
ATARI INCORPORATED
14600 Winchester Boulevard
Los Gatos, California 95030

TITLE: SCHEMATIC, SPRINT 2

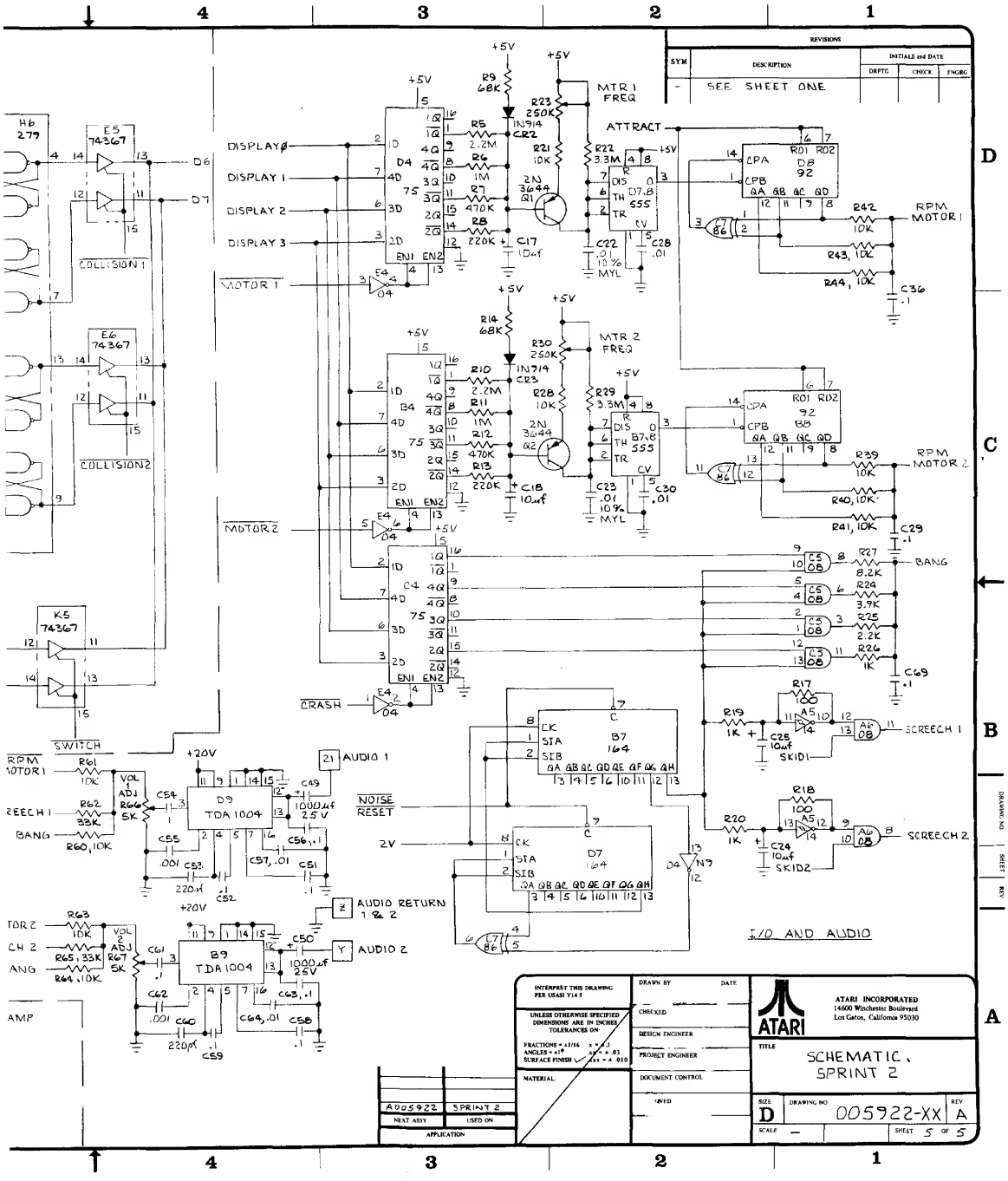
SIZE D | DRAWING NO 005922-XX | REV A

SCALE - | SHEET 4 OF 5

DRAWING NO. | SHEET | REV



8
7
6
5
D
C
B
A
+5V
R85 27
F8,9 SW2
ADR5
SPARE
SPARE
3RD 2
3RD 1
2ND 2
2ND 1
1ST 2
1ST 1
F9 9312
330 8 PLACES
ADRØ
ADR1
ADR2
ADR4
TRAK SEL
START 2
START
SELF TEST
GAS 2
GAS 1
H9 9312
330 7 PLACES
ADR3
J9 156
P.R38
ADR1
ADRØ
F8-9 SW2
10 TIME 1
12 EXT PLAY
14 $ MODE 1
16 OIL SLICKS
9 TIME Ø
11 SPARE
13 $ MODE Ø
15 TRK CYC
J8,9 SW1
R45 330
A8 20
P.R38
N9 04
R46 330
BLACK PLAYFIELD
CAR 2
CAR 3 & 4
F8 00
F6 32
H6 279
E5 74367
COLLISION RESET 1
COLLISION 1
CAR 1
WHITE PLAYFIELD
COLLISION RESET 2
E6 74367
COLLISION 2
BLACK PLAYFIELD
ADR6
ADR7
M8 153
K5 74367
SWITCH
STEERING 1A
STEERING 1B
R59 10K
R58 10K
C44 .01
C45 .01
L9
M9 74
STEERING RESET 1
STEERING 2A
STEERING 2B
R54 10K
R56 10K
C47 .01
C46 .01
L8 74
STEERING RESET 2
R55 10K
R57 10K
1N4001
COIN SW. 1
COIN SW. 2
N.C.
NO
COM
10V
GND TO SW & STEER. BOARD
+5V TO STEERING BD
1 PLAYER LAMP
LAMP 1
R35 100
LAMP 2
R37 100
2 PLAYER LAMP
R84 220
TRACK SEL LMP
RPM MOTOR 1
R61 10K
SCREECH 1
R62 33K
BANG
R60, 10K
VOL 1 ADJ R66 5K
RPM MOTOR 2
R63 10K
SCREECH 2
R65, 33K
R64, 10K
VOL 2 ADJ R67 5K
C61
C62 .001


REVISIONS
SYM | DESCRIPTION | INITIALS and DATE: DRFTG, CHECK, ENGRG
- SEE SHEET ONE
DISPLAYØ
DISPLAY 1
DISPLAY 2
DISPLAY 3
MOTOR 1
MOTOR 2
CRASH
COLLISION 1
COLLISION 2
SWITCH
MTR 1 FREQ
MTR 2 FREQ
ATTRACT
RPM MOTOR 1
RPM MOTOR 2
BANG
SCREECH 1
SCREECH 2
NOISE RESET
AUDIO 1
AUDIO 2
AUDIO RETURN 1 & 2
AMP
I/O AND AUDIO
ATARI INCORPORATED
14600 Winchester Boulevard
Los Gatos, California 95030
SCHEMATIC, SPRINT 2
005922-XX
SPRINT 2

ATARI

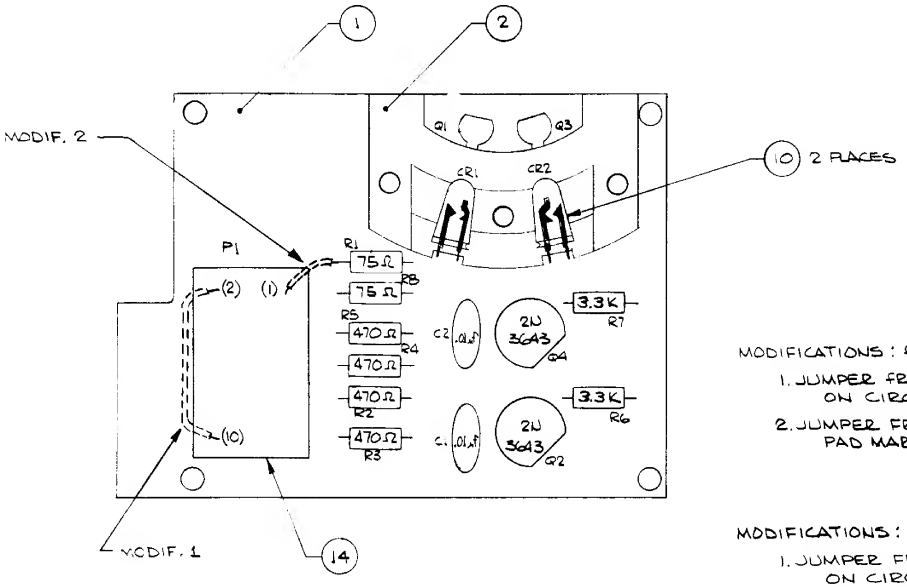
Job Title	RACETRAK STEERING PCB ASSY	Dwg. P/L 000607

Parts List Specification sheet 1 of 1

Drawn		
Checked	Mech. Eng.	Rev.
Proj. Eng. MF	Elec. Eng.	M

Rev.	Description	Apprv.	Rev.	Description	Apprv.
H	Redesigned				
J	Rev per ECN 397				
K	Rev per ECN 457				
L	Rev per ECN 601				
M	Rev per ECN 1531				

Item	Part. No.	Qty.	Description
1	000614	1	Printed Circuit Board (E)
2	001092	1	Light Mount
3	001151	Ref	Schematic Diagram
4	11750/10-5750	2	Resistor, Comp., 75 ohm, ¼ watt, 5%
5	11471/10-5471	4	Resistor, Comp, 470 ohm, ¼ watt, 5%
6	11332/10-5332	2	Resistor, Comp, 3.3Kohm, ¼ watt, 5%
7	34104 /27-101103	2	Capacitor, Ceramic, .01uf
8	70006/38-2N5777	2	Transistor, 2N 5777 (Photo Darlington)
9	70000/34-2N3643	2	Transistor, 2N 3643
10	71008/38-ME7124	2	Light Emitting Diode, I.R. ME 7124
11			
12			
13			
14	80089 /79-58005	1	Connector, 10 pin, PC Mount, Amp #1-380991
15	72-1212S	1	Screw, Machine, Pan Head Phil, #2-56 x 3/4 Lg.
16	75-042	1	Washer, Split Lock #2
17	75-912S	1	Nut, Hex, #2-56
18	003749	1	Retainer, Led Light Mount



REFER TO SCHEMATIC 001151

REVISIONS			
SYM	DESCRIPTION	INITIALS and DATE	
		DRFTG	
H	REDESIGNED	5-3-74	
J	REV. PER ECN 397	5-28-74	
K	REV. PER ECN 457	6-3-74	
L	REV PER ECN 601	7-16-74	
M	REV PER ECN 1531	7/8/75	

MODIFICATIONS: FOR 000614 REV J P.C. BOARDS

1. JUMPER FROM PIN 2 TO PIN 10 OF THE 10 PIN CONNECTOR, ON CIRCUIT SIDE OF BOARD.
2. JUMPER FROM PIN 1 OF THE 10 PIN CONNECTOR TO THE PAD MARKED +5V (END OF R1) ON CIRCUIT SIDE OF BOARD.

MODIFICATIONS: FOR 000614 REV K P.C. BOARDS.

1. JUMPER FROM PIN 2 TO PIN 10 OF THE 10 PIN CONNECTOR, ON CIRCUIT SIDE OF BOARD.

NEXT ASSY: A000598	USED ON: A000519	APPLICATION	

INTERPRET THIS DRAWING PER USASI Y14.5

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS ± 1/16 .X ± .1
ANGLES ± 1° .XX ± .03
SURFACE FINISH .XXX ± .010

MATERIAL: SEE PL 000607

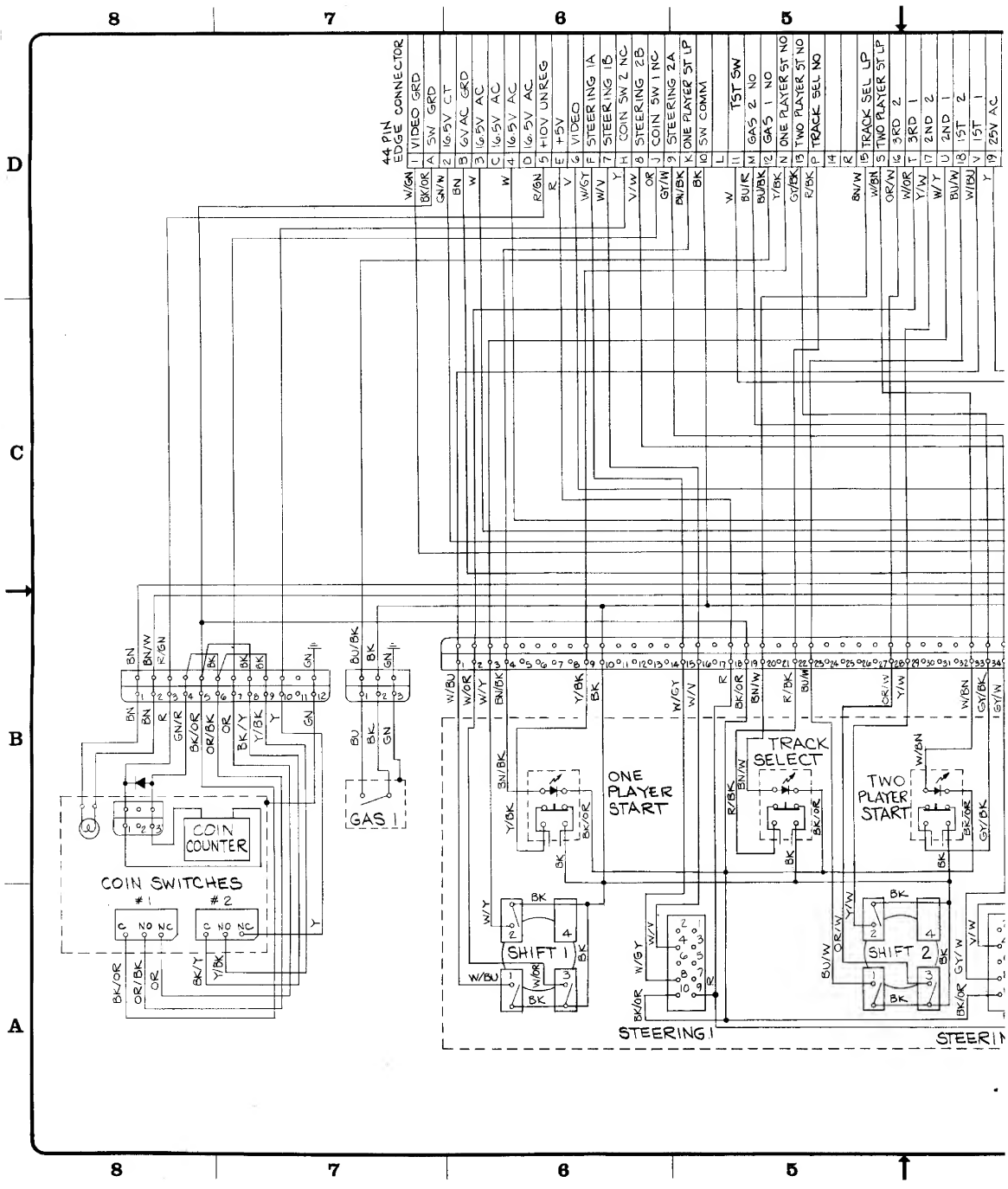
DRAWN BY — DATE: 5-6-74
CHECKED
DESIGN ENGINEER
PROJECT ENGINEER
DOCUMENT CONTROL

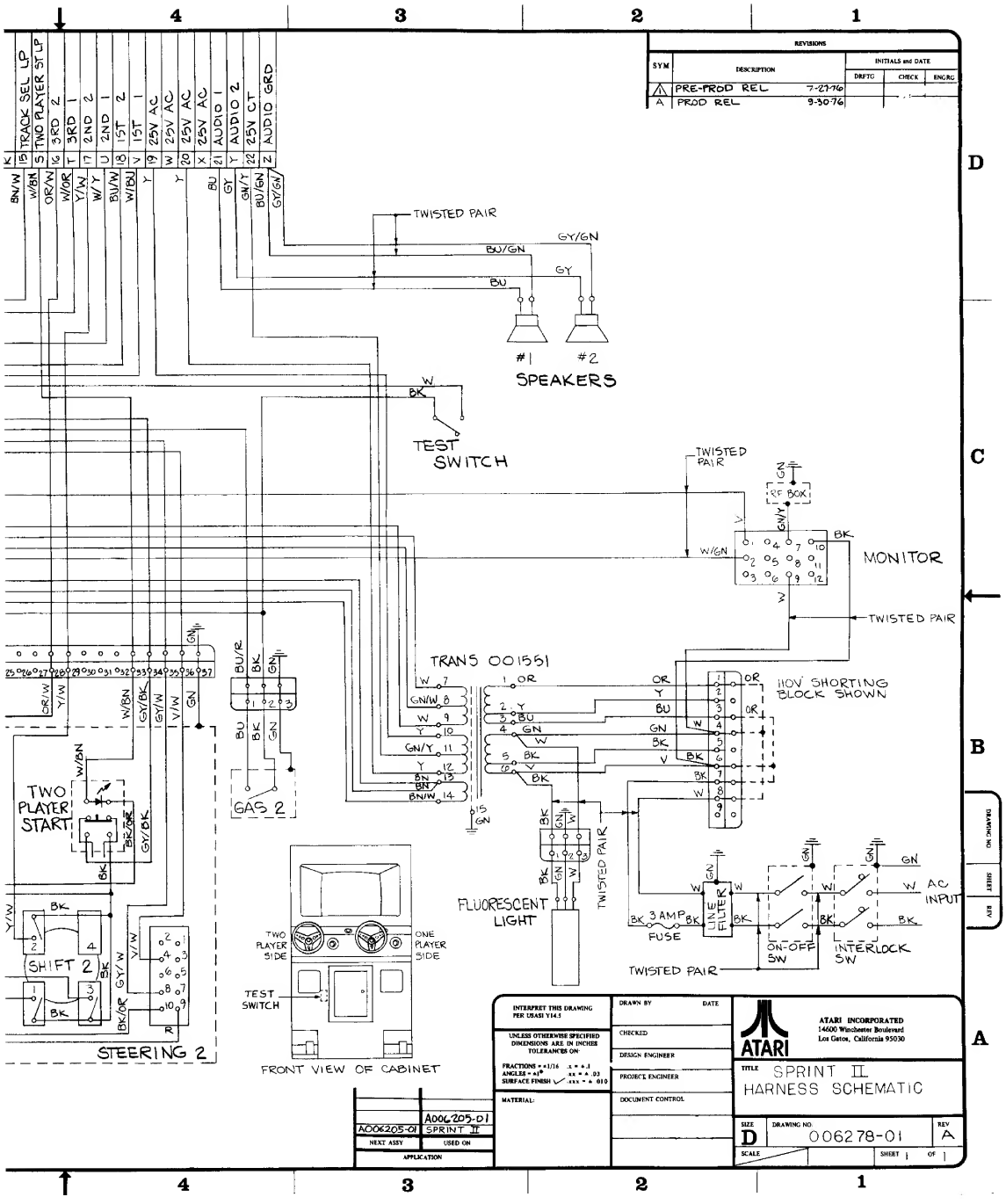
ATARI INCORPORATED
14600 Winchester Boulevard
Los Gatos, California 95030

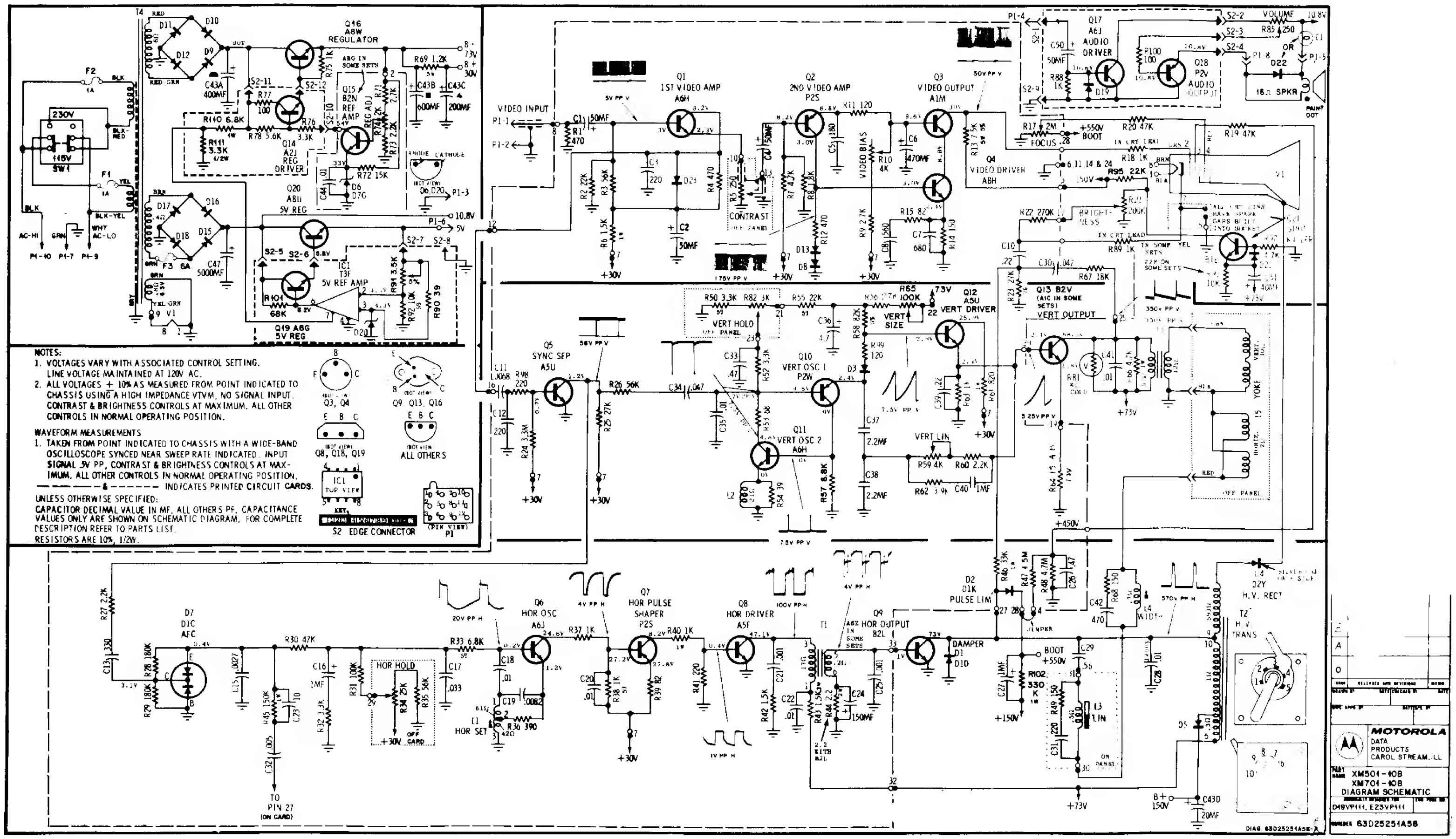
TITLE: ASSEMBLY STEERING BOARD

SIZE: B | DRAWING NO: A000607 | REV: M

SCALE: 2:1 | SHEET 1 OF 1


8
7
6
5
D
C
B
A
44 PIN EDGE CONNECTOR
1 VIDEO GRD
A SW GRD
2 16.5V CT
B 6V AC GRD
3 16.5V AC
C 16.5V AC
4 16.5V AC
D 16.5V AC
5 +10V UNREG
E +5V
6 VIDEO
F STEERING 1A
7 STEERING 1B
H COIN SW 2 NC
8 STEERING 2B
J COIN SW 1 NC
9 STEERING 2A
K ONE PLAYER ST LP
10 SW COMM
L
11 TST SW
M GAS 2 NO
12 GAS 1 NO
N ONE PLAYER ST NO
13 TWO PLAYER ST NO
P TRACK SEL NO
14
R
15 TRACK SEL LP
S TWO PLAYER ST LP
16 3RD 2
T 3RD 1
17 2ND 1
U 2ND 2
18 1ST 2
V 1ST 1
19 25V AC
Y
COIN COUNTER
COIN SWITCHES
#1
#2
GAS 1
ONE PLAYER START
TRACK SELECT
TWO PLAYER START
SHIFT 1
SHIFT 2
STEERING 1
STEERING 2


REVISIONS
SYM | DESCRIPTION | INITIALS and DATE | DRFTG | CHECK | ENGRG
A PRE-PROD REL 7-27-76
A PROD REL 9-30-76
TRACK SEL LP
TWO PLAYER ST LP
3RD 2
3RD 1
2ND 2
2ND 1
1ST 2
1ST 1
25V AC
25V AC
25V AC
AUDIO 1
AUDIO 2
25V CT
AUDIO GRD
TWISTED PAIR
GY/GN
BU/GN
GY
BU
#1
#2
SPEAKERS
TEST SWITCH
MONITOR
TRANS 001551
110V SHORTING BLOCK SHOWN
GAS 2
TWO PLAYER START
SHIFT 2
STEERING 2
FLUORESCENT LIGHT
3 AMP FUSE
LINE FILTER
ON-OFF SW
INTERLOCK SW
AC INPUT
TWO PLAYER SIDE
ONE PLAYER SIDE
TEST SWITCH
FRONT VIEW OF CABINET
INTERPRET THIS DRAWING PER USASI Y14.5
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON:
FRACTIONS ±1/16 .x ± .1
ANGLES ± 1° .xx ± .03
SURFACE FINISH .xxx ± .010
MATERIAL:
DRAWN BY DATE
CHECKED
DESIGN ENGINEER
PROJECT ENGINEER
DOCUMENT CONTROL
ATARI INCORPORATED
14600 Winchester Boulevard
Los Gatos, California 95030
TITLE SPRINT II
HARNESS SCHEMATIC
SIZE D
DRAWING NO. 006278-01
REV A
SCALE
SHEET 1 OF 1
A006205-01
SPRINT II
NEXT ASSY
USED ON
APPLICATION


NOTES:
1. VOLTAGES VARY WITH ASSOCIATED CONTROL SETTING. LINE VOLTAGE MAINTAINED AT 120V AC.
2. ALL VOLTAGES ± 10% AS MEASURED FROM POINT INDICATED TO CHASSIS USING A HIGH IMPEDANCE VTVM, NO SIGNAL INPUT. CONTRAST & BRIGHTNESS CONTROLS AT MAXIMUM. ALL OTHER CONTROLS IN NORMAL OPERATING POSITION.
WAVEFORM MEASUREMENTS
1. TAKEN FROM POINT INDICATED TO CHASSIS WITH A WIDE-BAND OSCILLOSCOPE SYNCED NEAR SWEEP RATE INDICATED. INPUT SIGNAL .5V PP, CONTRAST & BRIGHTNESS CONTROLS AT MAXIMUM. ALL OTHER CONTROLS IN NORMAL OPERATING POSITION.
& INDICATES PRINTED CIRCUIT CARDS.
UNLESS OTHERWISE SPECIFIED:
CAPACITOR DECIMAL VALUE IN MF, ALL OTHERS PF. CAPACITANCE VALUES ONLY ARE SHOWN ON SCHEMATIC DIAGRAM. FOR COMPLETE DESCRIPTION REFER TO PARTS LIST.
RESISTORS ARE 10%, 1/2W.
Q3, Q4
Q9, Q13, Q16
Q8, Q18, Q19
ALL OTHERS
IC1 TOP VIEW
S2 EDGE CONNECTOR
P1 (PIN VIEW)
Q46 A8W REGULATOR
Q15 B2N REF AMP
Q14 A2J REG DRIVER
Q20 A8U 5V REG
IC1 T3F 5V REF AMP
Q19 A6G 5V REG
VIDEO INPUT
Q1 1ST VIDEO AMP A6H
Q2 2ND VIDEO AMP P2S
Q3 VIDEO OUTPUT A1M
Q4 VIDEO DRIVER A8H
VIDEO BIAS
CONTRAST
Q17 A6J AUDIO DRIVER
Q18 P2V AUDIO OUTPUT
VOLUME
SPKR
FOCUS
BOOT
BRIGHTNESS
V1
Q5 SYNC SEP A5U
VERT HOLD
Q10 VERT OSC 1 P2W
Q11 VERT OSC 2 A6H
VERT SIZE
Q12 A5U VERT DRIVER
VERT LIN
Q13 82V VERT OUTPUT
YOKE
D7 D1C AFC
HOR HOLD
Q6 HOR OSC A6J
HOR SET
Q7 HOR PULSE SHAPER P2S
Q8 HOR DRIVER A5F
Q9 HOR OUTPUT 82L
DAMPER
D2 D1K PULSE LIM
WIDTH
LIN
D4 D2Y H.V. RECT
T2 H.V. TRANS
DIAG 63D25251A58-A
MOTOROLA
DATA PRODUCTS
CAROL STREAM, ILL
PART NAME XM501-40B
XM701-40B
DIAGRAM SCHEMATIC
D18VP111, E23VP111
NUMBER 63D25251A58